NAS8-21164

DEVELOPMENT OF SSB/DSB AUXILIARY TIME DIVISION MULTIPLEXER AND DEMULTIPLEXER

FINAL REPORT

FEBRUARY 1968

Prepared For

George C. Marshall Space Flight Center

National Aeronautics and Space Administration

Huntsville, Alabama 35812

Prepared by

MARTIN MARIETTA CORPORATION

DENVER, COLORADO

MCR-68-57

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George C. Marshall Space Flight Center

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DENVER, COLORADO

ABSTRACT

This report describes the results of the development contract, NAS8-21164, for an SSB/DSB auxiliary time division multiplexer prototype and a demultiplexer breadboard. This contract was performed for the George C. Marshall Space Flight Center of the National Aeronautics and Space Administration of Huntsville, Alabama by Martin Marietta Corporation, Denver Division. The multiplexer time multiplexes up to 80 subchannels into 20 channels and provides a pseudo random sync code. The demultiplexer uses the pseudo random sync code to demultiplex any 3 channels into the original subchannels and provides identification for the time each subchannel is active and a sync code error signal.

FOREWARD

This report describes the results of the development program of an SSB/DSB Auxiliary Time Division Multiplexer prototype and a Demultiplexer breadboard conducted by Martin Marietta Corporation for the George C. Marshall Space Flight Center of the National Aeronautics and Space Administration at Huntsville, Alabama. This report is submitted under Exhibit A, Part I, Phase V of the statement of work for Contract NAS8-21164.

CONTENTS

Figure

I. INTRODUCTION AND SUMMARY

The Martin Marietta Corporation has developed a SSB/DSB auxiliary time division multiplexer and demultiplexer for the George C. Marshall Space Flight Center under contract number NAS8-21164. This contract was performed in the period between June 14, 1967 and February 19, 1968. The multiplexer prototype was designed, constructed and tested in accordance with the requirements of Drawing GC 110379 as amended. The demultiplexer breadboard was designed, constructed and tested in accordance with the requirements of Drawing GC 110380.

This final report describes the principles of operation of the multiplexer and demultiplexer, the mechanical construction of the multiplexer and demultiplexer, and usage considerations for the multiplexer and demultiplexer. The multiplexer prototype was successfully tested under the environments listed in the drawing. Both the multiplexer and demultiplexer were tested electrically to the drawing requirements. The results of these tests are given in the test report MCR-68-56 and were performed using the test procedure, drawing number 21164-5. The operating instructions for both units are in the operating manual, MCR-68-38.

The SSB/DSB auxiliary time division multiplexer can multiplex up to 80 subchannels of data onto 20 channels. Each pair of output channels can have 2, 4 or 8 subchannels multiplexed on them, i.e. 1, 2 or 4 per channel, but selection is made in two channel increments. When two subchannels are multiplexed, each subchannel is monitored alternately for 4 seconds; with four subchannels, the subchannels are monitored for 2 seconds sequentially. The frequency response of each channel is flat from dc to 3000 Hz for signal levels up to 5 volts peak-to-peak. The multiplexer operates from 28 vdc $\pm$ 15% power and is dc isolated from the power source. The multiplexer produces a pseudo-random sync code that contains all the information necessary to synchronously demultiplex and identify the data.

The SSB/DSB auxiliary time division demultiplexer accepts 20 multiplexed channel inputs from the multiplexer and simultaneously demultiplexes any three channels into 1, 2 or 4 subchannels using the information contained in the sync code. It also provides a signal for each subchannel to indicate when it is active. An error signal is also generated if the sync signal received does not contain the proper sync codes. The demultiplexer is rack mounted and operates from 117 volt, single phase, 60 Hz power.

II. PRINCIPLES OF OPERATION

A. GENERAL

The SSB/DSB auxiliary time division multiplexer and demultiplexer are companion pieces of equipment. The multiplexer is designed to time multiplex up to 80 subchannels into 20 channels. The subchannels are commutated onto the channel outputs as follows: one subchannel can be monitored continuously; two subchannels can be commutated alternately with each subchannel monitored for

4 sec., and four subchannels can be commutated in sequence with each subchannel monitored for 2 sec. The selection of 1, 2 or 4 subchannel commutation is performed two channels at a time by selection of interchangeable modules.

The magnitude of transients that could occur at the time of commutation is minimized by modulating the gain of the amplifiers downward to produce a trapezoidal modulation on the amplifier's output waveform. In addition, the effect of this modulation on external equipment is minimized by commutating the channels in sequence so that only one channel has its gain reduced at any time. The methods of achieving these operations are discussed in detail in the amplifier and sequence generator respectively.

The multiplexer generates a synchronization signal to allow the demultiplexer to synchronously demultiplex any three channels into the original subchannels -- either 1, 2 or 4 as indicated by the code words that form the synchronization signal. The synchronization signal also enable synchronization of the decommutation and identification of each subchannel. The synchronization signal consists of an 8 sec. repetetive sequence of 80 20-bit words that are biphase coded using a 400 Hz square wave. This provides easy bit sync recovery and a 200 Hz lower limit of the significant signal power content. The code words used are six "comma free" words with three words being the complements of the other three. Comma free means that there are no combinations of the last part of any word and the first part of any word that are identical to any word. One of the three complements is used to indicate the beginning of each 8 sec. cycle and also to indicate if channel 1 is continuous or commutates 2 or 4 subchannels. The other three words are used to indicate the commutation of each of the other 19 channels 4 times in each cycle and also 3 more times for channel 1.

The SSB/DSB auxiliary time division demultiplexer receives the twenty commutated data channels and the synchronization signal. It can demultiplex any three channels at once and identify the subchannels using the information contained in the synchronization signal. Bit sync is obtained by regenerating the clock from the level transistion that <u>always</u> occurs in the middle of each bit of the synchronization signal. The regenerated clock shifts the demodulated sync signal into a 20 bit shift register. The shift register is continuously monitored for any of the six code words. Cycle synchronization occurs when any of the three complement words are detected. Word synchronization is easily obtained since a correct code in the shift register lasts only one bit. Sequence regeneration is obtained using a 20 stage ring counter that counts word sync and is reset by cycle sync.

The above information is used to decommutate the 3 channels selected by the demultiplexer's rotary channel selector switches. The demultiplexer outputs are the decommutated subchannels and a synchronizing signal to indicate each active subchannel. An error signal is also produced when a word is not detected every 20 bits.

B. MULTIPLEXER

The multiplexer is basically a group of 20 switch sets and amplifiers and the Control Circuitry to provide properly timed control signals. A synchronization signal required to properly demultiplex the data signals is also provided. Figure II-1, shows the multiplexer block diagram.

1. Sequence Generator

The sequence generator provides the basic timing for operation of the subcommutating switches and for the synchronization code generator. Figure II-2 shows the block diagram of the sequence generator. The circuitry is composed of integrated circuit logic devices except for the 1600 Hz oscillator which is a unijunction transistor oscillator. The 1600 Hz clock provides the basic timing for both the switching sequence and the synchronization code generator.

The 20 multiplexer channels are capable of multiplexing 1, 2, or 4 subchannels depending on the type of channel module in use. Thus up to 80 subchannel signals can be multiplexed to the 20 output channels. The total commutation cycle for any one channel is 8 seconds, thus a channel which commutates two subchannels selects each subchannel signal for 4 seconds of the 8 second period. Similarly for a channel commutating four subchannels each subchannel signal is selected for 2 sec of the 8 second period.

The sequence generator provides switching signals to each channel in sequence so that only one channel is commutating from one subchannel to another during any switching period. To allow up to 80 subchannels to be commutated into 20 channels, the sequence generator provides 80 separate switching periods at intervals of 0.1 seconds. Each channel is provided with 4 switching signals in each 8 second commutation cycle. The channel module uses these signals to commutate 4 subchannels or two subchannels according to the module used. No switching is done on channel modules having only one subchannel input per channel. The 80 switching periods are obtained from a 20 stage ring counter driven by a 10 Hz signal. The ring counter completes its count every 2 seconds or 4 times during each 8 second commutation cycle, such that a pulse of 0.1 sec. duration occurs every 2 seconds at each stage of the ring counter as shown in Figure II-3.

Each output of the 20 stage counter R_1 thru R_{20} (R_n) controls the subchannel switches for the respective channels 1 thru 20. The two-subchannel module switches with every second R_n pulse and the four-subchannel module switches with every R_n pulse. Thus the subchannel signals are properly sequenced to the channel output amplifier. Switching waveforms for a two and four subchannel channel are shown in Figure II-3.

In order to avoid high frequency switching transients on channel outputs the multiplexer channel amplifier gain is modulated to control the fall time of the subchannel signal turned off and the rise time of the subchannel signal turned on. Channel turn off is started 10 milliseconds before commutation takes place after which an additional 10 milliseconds is used in the turn on

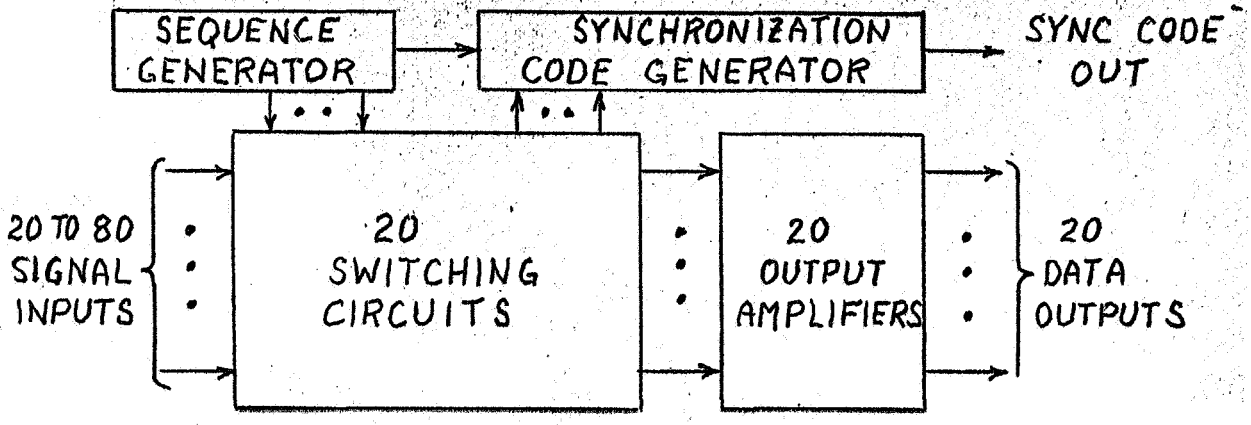


FIGURE II-1, MULTIPLEXER BLOCK DIAGRAM

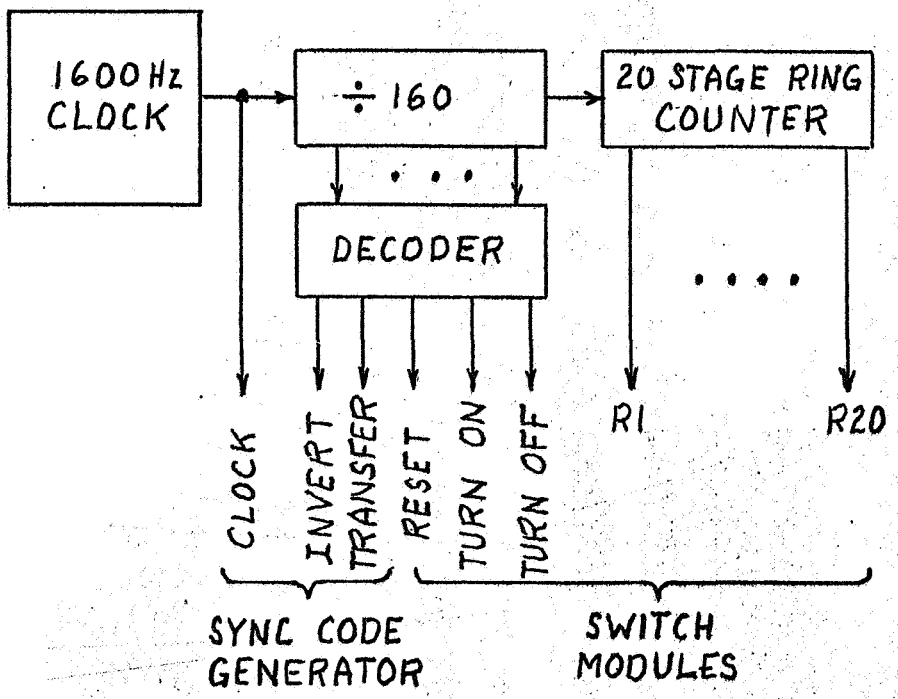


FIGURE II-2, SEQUENCE GENERATOR BLOCK DIAGRAM

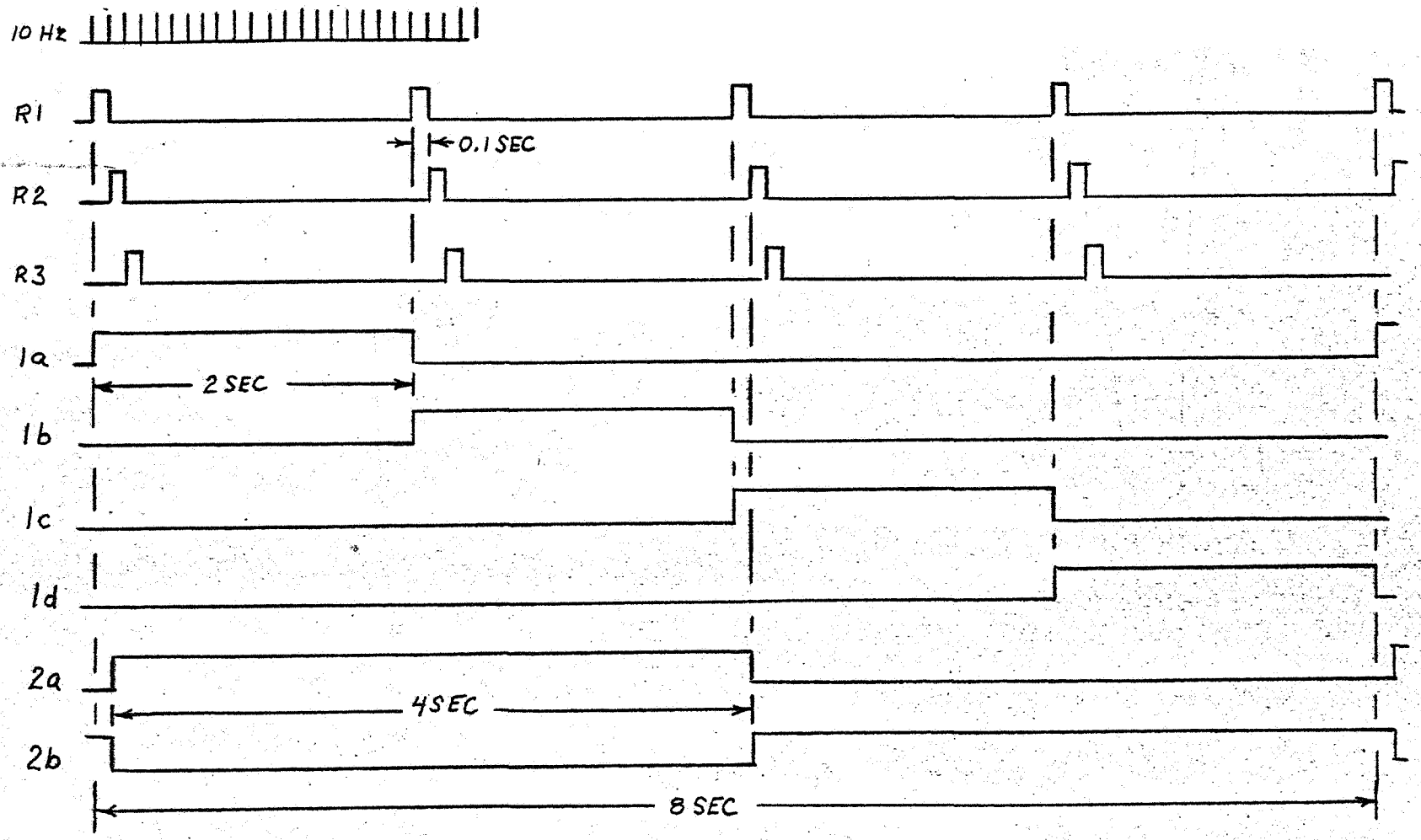


FIGURE II-3, SUBCHANNEL TIMING

of the succeeding subchannel signal. The 10 millisecond pulses for the turn off and turn on control are generated every 0.1 seconds by the sequence generator and are shown in Figure II-3. Each channel module uses these signals and its respective R_n to control its turn off and turn on. Operation of the gain control circuitry is discussed in the amplifier description.

The sequence generator also generates a reset signal every 8 seconds for the counters and the commutating control in each channel.

The logic diagram for the sequence generator is shown in Figure II-4. The waveforms generated by the sequence generator are shown in Figure II-5. The 1.6 KHz clock signal is divided to 200 Hz by the first three flip-flops. The next three are connected as a feed back counter to divide the 200 Hz signal by 5 to 40 Hz. The next two flip-flops divide the 40 Hz to 10Hz. The turn off control pulse and the turn on control pulse are decoded from these dividers. It will be noted that the 10 Hz signal used to drive the 20 stage ring counter occurs 5 milliseconds before the turn off signal goes positive. Thus the R_n pulses occur before actual commutation is to take place. This is done to allow the R_n pulse to be used to gate the proper T off and T on pulses into the proper channel amplifier. The turn on signal is then used to initiate the subchannel switch. The 20 stage ring counter is designed to be self reseting as follows.

The $\bar{Q}$ output of the stages R_1 - R_{19} are connected to a 19 input NAND gate which controls the feedback around the ring. As long as the $\bar{Q}$ output of any of the R_1 to R_{19} stages is false the flip-flop composed of cross coupled gates remains reset and transfers reset signals into the first stage. As soon as the first 19 stages are reset, the 20th stage is set, the cross-coupled gate flip-flop is set and enables the J input of the R_1 flip-flop. The 21st clock pulse sets R_1 flip-flop to the true state. The flip-flop made up of the cross-coupled gates is synchronized by the T off pulse. This pulse also gates out the sync invert command pulse from the divide-by-four flip-flops, A26. These waveforms are shown in Figure II-6. Also shown is the reset pulse generated every 8 seconds, and the sync transfer pulse which will be discussed with the sync code generator.

2. Synchronization Code Generator

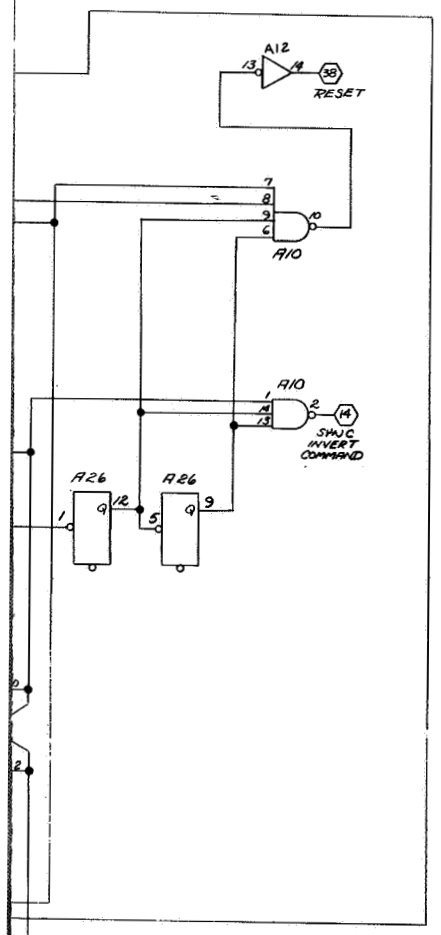
The synchronization code generator produces a pseudorandom code that contains the information to identify each channel and how each channel is commutated. This signal consists of a series of 80 twenty-bit codes every eight seconds. The code clock frequency is 200 Hz. Each of the twenty channels has 4 of the 80 codes associated with it. These four codes occur at the same times as R_1 through R_{20} for channels 1 through 20 respectively. Use of the six pseudorandom codes is as follows: code 1 is used to identify a channel with no commutation, code 2 is used to identify a channel that is commutated with two subchannels, and code 4 is used to identify a channel that is commutated with four subchannels. The complement of these three codes is used to identify channel 1 at the beginning of each eight-second sequence.

The block diagram of the synchronization code generator is shown in Figure II-7. The internal connections of each switch module connect the preceding channel signal (R_{n-1}) to the 1-, 2-, or 4-input depending on whether it is a one channel or a two or four subchannel switch module. This signal and the

PINS CONNECTED TO Vcc		PINS CONNECTED TO GROUND	
FUNCTIONAL DESIGNATION	PIN NUMBER	PIN NUMBER	TYPE
A1	1,4,6,7,12,13	11	SN5420
A2	2,3,4,6,7,10,14	11	SN 5473
A3	2,3,4,6,14	11	"
A4	2,4,6	11	"
A5	2,4,6	11	"
A6	1,4,6,7,8,12,13	11	SN5440
A7	1,4,6,7,13,14	11	SN5440
A8	4,12	11	SN5410
A9	4,6	11	SN5430
A10	4,12	11	SN5420
A12	2,4,6,12	11	SN5400
A13	2,4,6	11	SN5473
A14	4	11	SN5430
A15	2,4,6	11	SN5473
A16	2,4,6	11	"
A17	4	11	SN5430
A18	2,4,6	11	SN5473
A19	4,5,7	11	SN5430
A20	2,4,6	11	SN5473
A21	2,4,6	11	"
A22	2,4,6	11	"
A23	2,4,6	11	"
A24	2,4,6	11	"
A25	2,4,6	11	"
A26	2,3,4,6,7,10,14	11	"
A11	1,4,8,9,14	11	SN5420

PINS CONNECTED TO Vcc		PINS CONNECTED TO GROUND	
FUNCTIONAL DESIGNATION	PIN NUMBER	PIN NUMBER	TYPE
A1	1,4,6,7,12,13	11	SNJ5420
A2	2,3,4,6,7,10,14	11	SNJ5473
A3	2,3,4,6,14	11	"
A4	2,4,6	11	"
A5	2,4,6	11	"
A6	1,4,6,7,8,12,13	11	SNJ5440
A7	1,4,6,7,13,14	11	SNJ5440
A8	4,12	11	SNJ5410
A9	4,6	11	SNJ5430
A10	4,12	11	SNJ5420
A12	2,4,6,12	11	SNJ5400
A13	2,4,6	11	SNJ5473
A14	4	11	SNJ5430
A15	2,4,6	11	SNJ5473
A16	2,4,6	11	"
A17	4	11	SNJ5430
A18	2,4,6	11	SNJ5473
A19	4,5,7	11	SNJ5430
A20	2,4,6	11	SNJ5473
A21	2,4,6	11	"
A22	2,4,6	11	"
A23	2,4,6	11	"
A24	2,4,6	11	"
A25	2,4,6	11	"
A26	2,3,4,6,7,10,14	11	"
A11	1,4,8,9,14	11	SN5420

ITEM	ISSUE	REVISION RECORD	DATE	APPROVED
A		REVISED R1 VALUE	10/8	C.W.H.



NOTES

1. REFERENCE DESIGNATION USED A1 THRU A26, Q1, R1 THRU R4, C1 AND C2.
2. ALL RESISTANCE VALUES ARE IN OHMS.
3. PRINTED WIRING ASSEMBLY 21164-25
   PRINTED WIRING BOARD 21164-3C
   PRINTED WIRING MASTER 21164-45

MARTIN MARIETTA CORPORATION
DENVER DIVISION
P.O. BOX 179
DENVER, COLORADO

ELECTRICAL SCHEMATIC
SEQUENCE GENERATOR

J 04236 21164-55

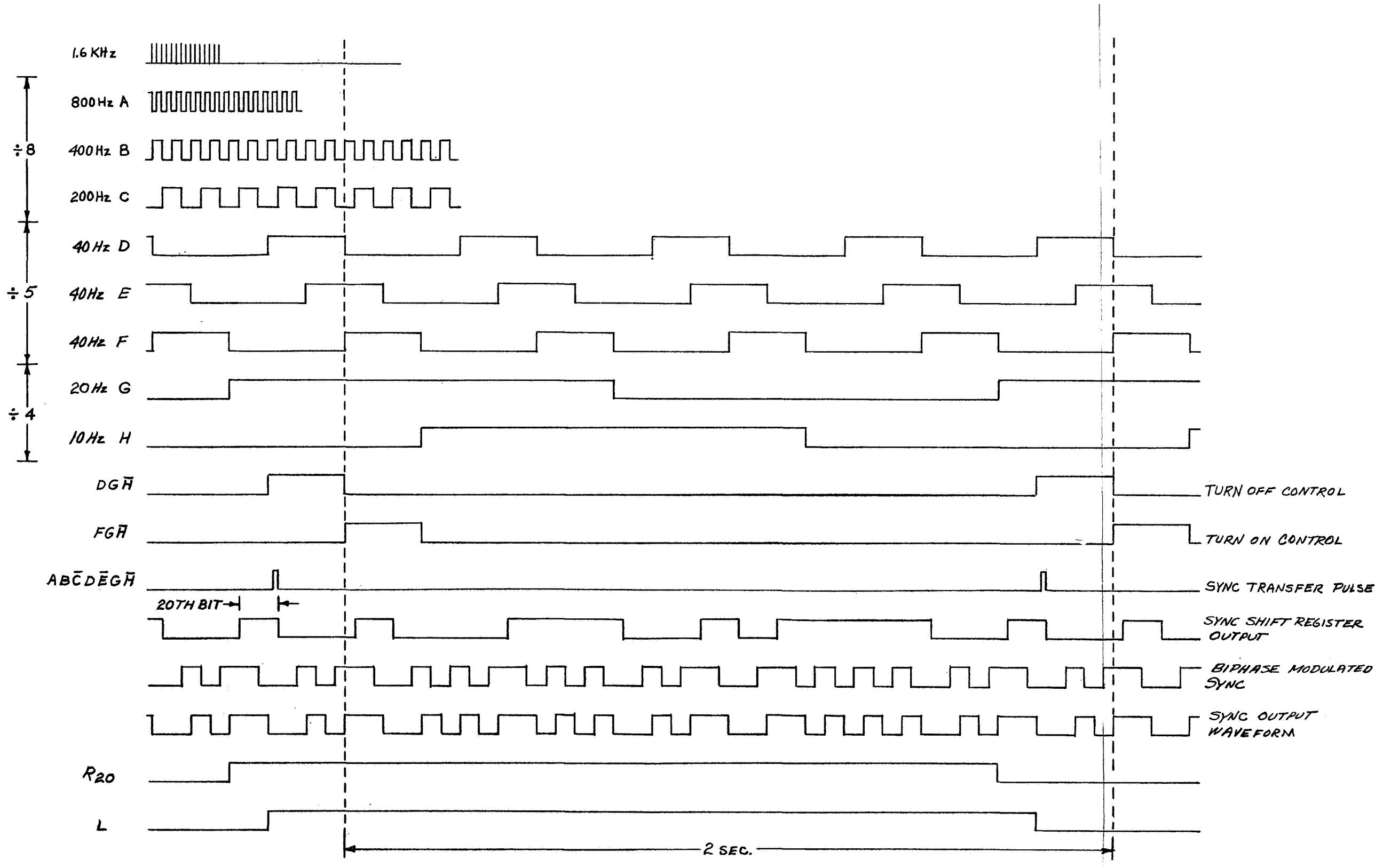


FIGURE II-5
MULTIPLEXER WAVEFORMS

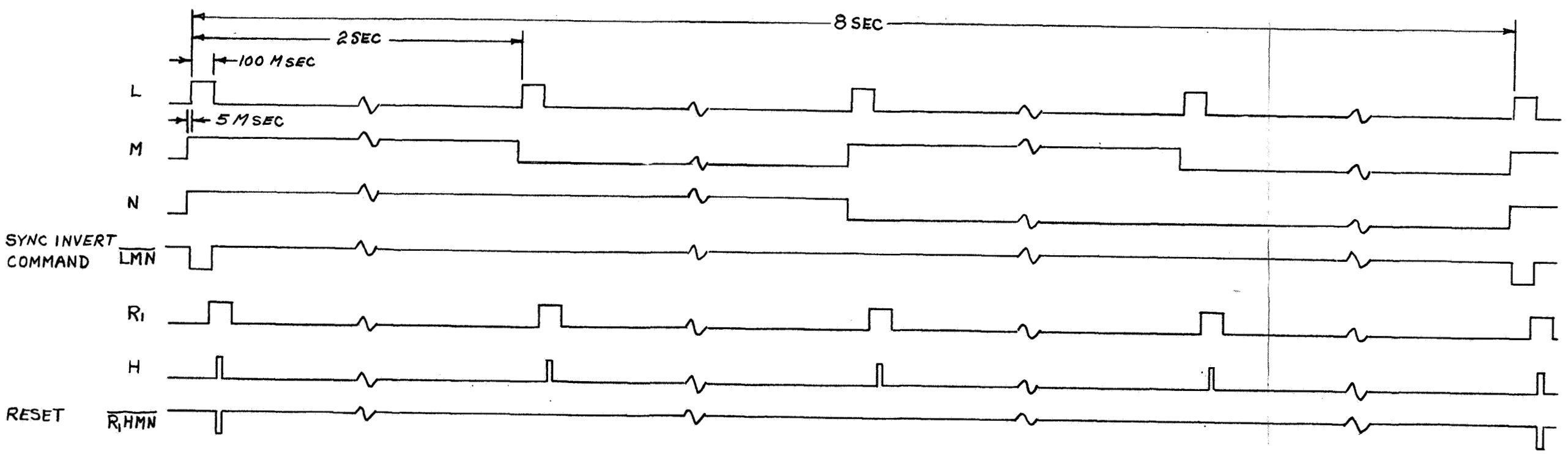


FIGURE II-6

SYNC INVERT COMMAND AND RESET WAVEFORMS

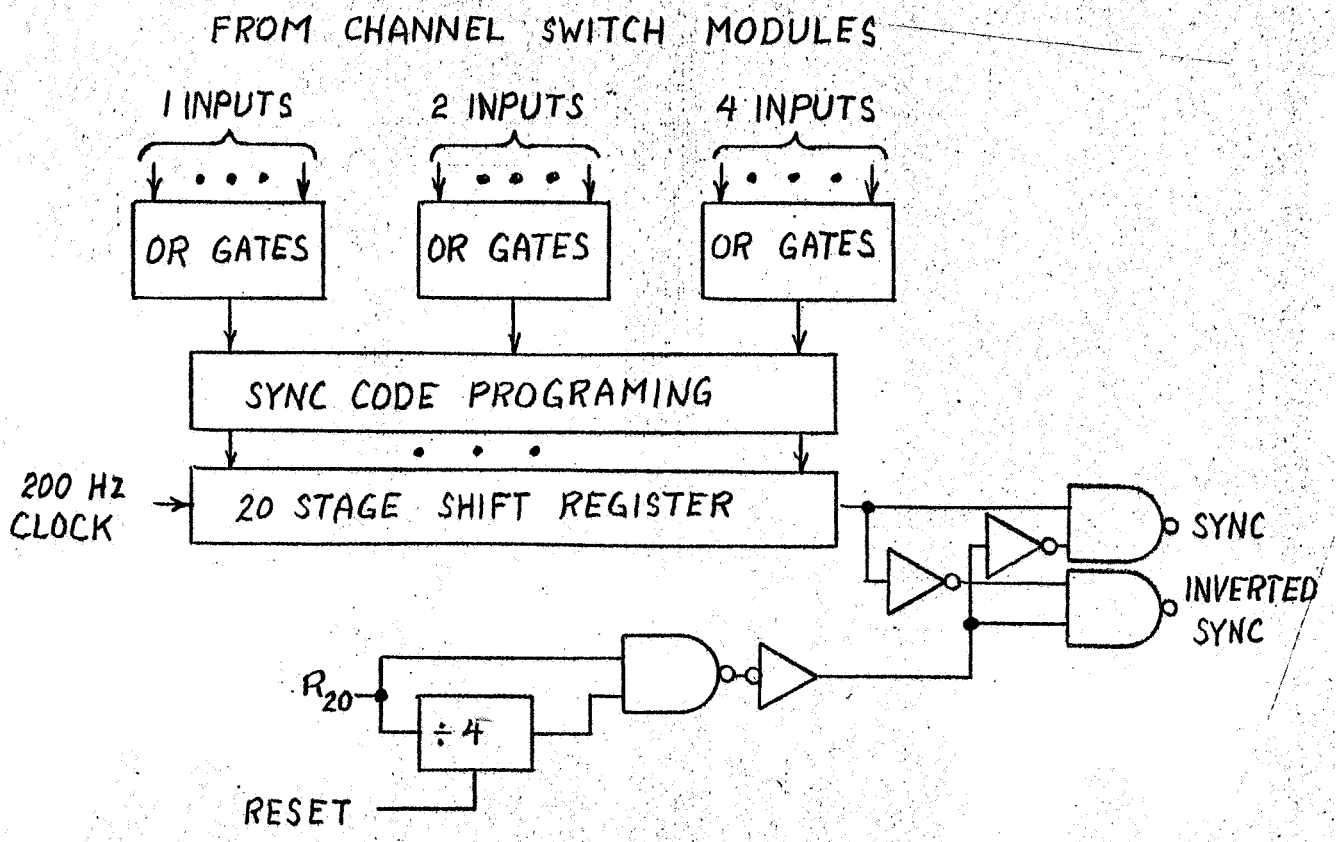


FIGURE II-7
SYNCHRONIZATION CODE GENERATOR
BLOCK DIAGRAM

sync transfer pulse then sets the one, two or four code into the 20-stage shift register where it is shifted serially out to the synchronization output. Logic is also provided so that every fourth R_{20} pulse inverts the synchronization output to provide the complement for identification of the beginning of each eight-second period.

The sync code generator logic is implemented entirely of integrated circuits and is constructed on two plug in boards. The "OR" gates are shown in Figure II-8. This logic is somewhat different than that illustrated in Figure II-4 in that the 1's inputs are not used. Since the absence of either a 2 or 4 indicates that a 1 sync code should be generated a separate OR gate for the "1"s is not necessary. Thus when the 2 or 4 outputs are low the "1"s output is high.

These three signals feed the sync code busses on the sync code generator board shown in Figure II-9.

It should be noted that the 4's OR gate has 20 inputs and the 2's OR gate 10 inputs. The 2 subchannel module's provide for OR ing of two channel signals before being transmitted to the Sync Code OR gate board.

The sync code generator board is constructed such that various sync codes could be hard wired on the programable portion of the board. The sync codes chosen for the prototype are shown in Figure II-10.

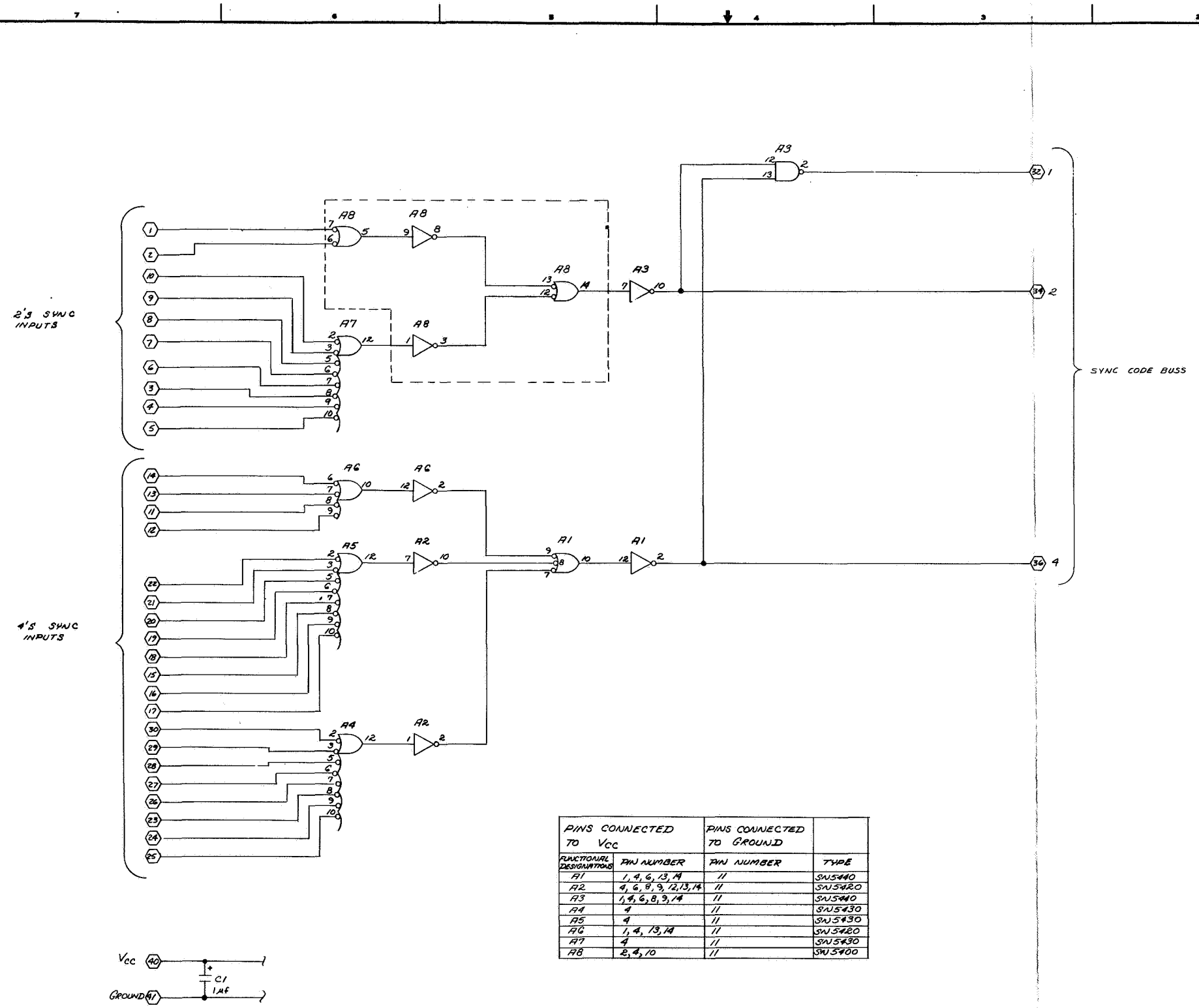
SYNCHRONIZATION CODES

Bit No	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
"1"	0	0	1	0	0	0	1	1	1	0	0	1	0	1	1	1	1	0	0	1
"2"	0	1	1	1	0	1	1	0	1	0	0	0	0	0	1	0	1	0	1	1
"4"	0	0	0	1	0	0	0	0	1	1	1	0	0	1	0	0	1	1	1	1

Figure II-10

These words and their complements are "comma free" which is a requirement of this system.

The sync transfer pulse shifts the code words into the 20 stage shift register once every 0.1 sec. The 200 Hz clock goes positive as the sync transfer pulse goes low. This shifts the 1st bit into the first stage of the D type flip-flop A23 thru the exclusive OR gate A22. If the sync invert command signal is true the 1st bit is inverted as it is shifted into A23. The second half of A22 is used to Biphase modulate the sync code at a 200 Hz clock rate. This signal is then clocked thru the second half of A23 by a 400 Hz signal to delay the sync code by 1.25 ms and to ensure that any switching transients introduced by the biphase modulation technique are eliminated. The sync code generator output impedance is approximately 50 ohms. The 20th bit of the sync code is generated 15 milliseconds before commutation actually occurs to allow sufficient time for the demultiplexer to recover sync information for commutation. The



PINS CONNECTED TO Vcc		PINS CONNECTED TO GROUND	
FUNCTIONAL DESIGNATIONS	PIN NUMBER	PIN NUMBER	TYPE
A1	1, 4, 6, 13, 14	11	SN5440
A2	4, 6, 8, 9, 12, 13, 14	11	SN5420
A3	1, 4, 6, 8, 9, 14	11	SN5440
A4	4	11	SN5430
A5	4	11	SN5430
A6	1, 4, 13, 14	11	SN5420
A7	4	11	SN5430
A8	2, 4, 10	11	SN5400

NOTES
1. REFERENCE DESIGNATIONS USED
   A1 THRU A8, C1
2. REFERENCE DRAWINGS
   PRINTED WIRING ASSEMBLY 21164-27
   PRINTED WIRING BOARD 21164-37
   PRINTED WIRING MASTER 21164-47

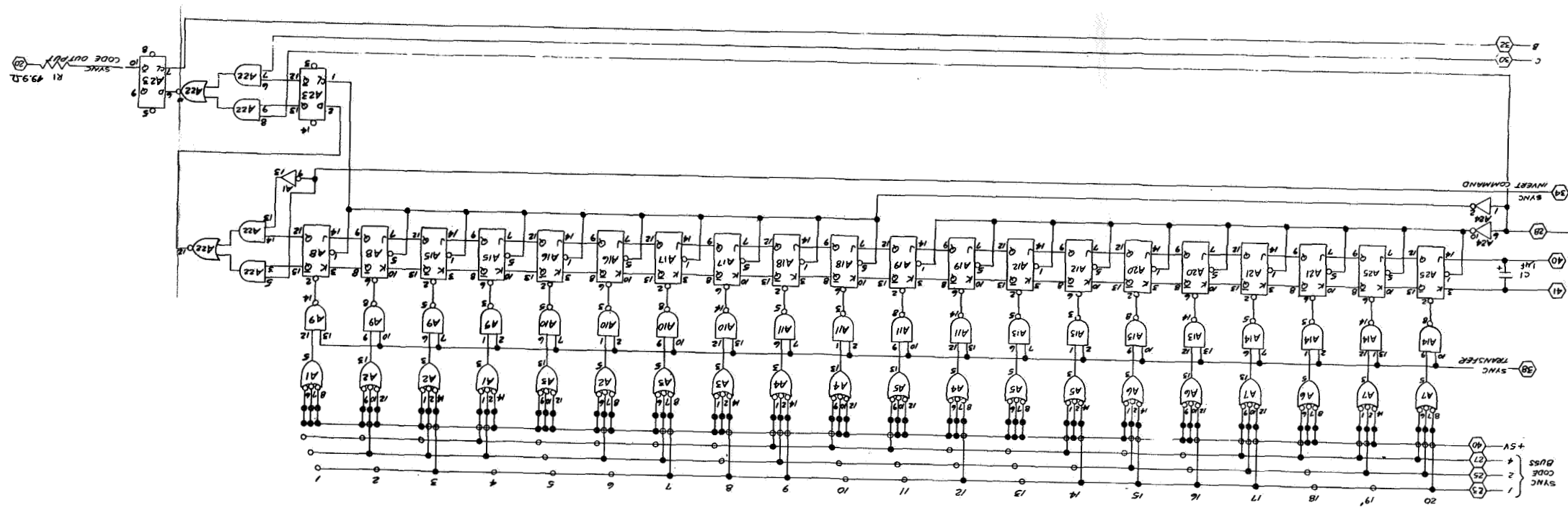
REVISIONS

SYM.	ZONE	DESCRIPTION	DATE	APPROVED

MARTIN MARIETTA CORPORATION
DENVER DIVISION P.O. BOX 179 DENVER, COLORADO

ELECTRICAL SCHEMATIC
SYNC CODE GENERATOR
"OR" GATES

SIZE E | CODE IDENT. NO. 38997 | 21164-57



PINS CONNECTED TO Vcc	PINS CONNECTED TO GROUND	
FUNCTIONAL DESIGNATIONS	PIN NUMBER	TYPE
A1	4 to 5,12	SN5490
A2 THRU A7	4	SN7410
A8, A11, A14, A15 THRU A20	4	SN5400
A9, A12, A13 THRU A21	4	SN5473
A22	4	SN5451
A23	5,6,9,8,12,4	SN5474
A24	4,8,9,8,12,3,8,4	SN5440
A25	4 & 14	SN5473

NOTES

1. FUNCTIONAL DESIGNATIONS USED AT THRU A25, C1, R1
2. REFERENCE DRAWINGS
   PRINTED WIRING ASSEMBLY 2114-56
   PRINTED WIRING BOARD 2114-36
   PRINTED WIRING MASTER 2114-46

time relationships of the sync code is shown in Figure II-5.

3. Subchannel Switches

Switches are required for the time sharing of two or four subchannels within a main channel. The switches isolate respective subchannels from each other to the extent that intermodulation caused by a 2.5-volt (peak-to-peak), 1.5-kHz signal applied to all channels but one will not result in a signal on the unexcited channel greater than 50 decibels below the 2.5-volt level. Insulated gate transistors (MOS) have adequate off-to-on impedance ratios and low enough shunt capacities to meet this requirement. MOSs are also available in the enhancement or normally off mode, which makes them ideal for use as commutating switches. Figure II-11 shows the circuit for a typical switch and driver.

The dual MOS on the input is arranged so that the 100K resistor is either grounded or connected to the low impedance of the amplifier input. Thus the system input impedance is 100K whether the input is connected to the amplifier or not. The MOS driver circuit requires the input to be grounded to connect the signal to the amplifier input. All three transistors in the driver are non-conducting unless the switch is on. Figures II-12 & 13 shows the logic diagrams for generation of the switch driver input signals for the two and four subchannel commutation. Figure II-14 shows the input and output waveforms for the two and four subchannel switch driver logic.

For the two subchannel switch driver logic, R_n toggles the flip-flop A_s. Thus R_n and the output of A_s select every second turn off and turn on pulse associated with the channel. B_s changes state every 4 seconds and the Q & $\bar{Q}$ signals drive the two MOS switch drivers. It should be noted that the flip-flop B_s is synchronized by the turn on pulse. Both flip-flops are reset every 8 seconds by the reset pulse.

The four subchannel switch driver is quite different in that the flip-flops A_s and B_s are connected as a two stage switch tail ring counter which divides the input by four. The input to the counter is the turn on pulse selected by R_n. The four states of the counter are selected by the four two input NAND gates and drive the four MOS switch drivers. The subchannel turn off and turn on signals are selected by R_n and occur every 2 seconds. Both flip-flops are reset every 8 seconds by the reset pulse.

4. Channel Amplifiers

A nominal unity gain, inverting amplifier is provided in each channel to perform decoupling and impedance matching. The amplifier consists of an integrated circuit operational amplifier with an external field effect transistor (FET) input stage. The FET input stage reduces the input offset current and current drift.

The open-loop gain of the amplifier is high (> 10,000) so that negative feedback is used to stabilize the gain to $\pm$1.0% and the amplifier linearity to $\pm$0.1% over the frequency range of DC to 3kHz. Also the negative feedback provides a very low dynamic output impedance. A fifty ohm series resistor protects

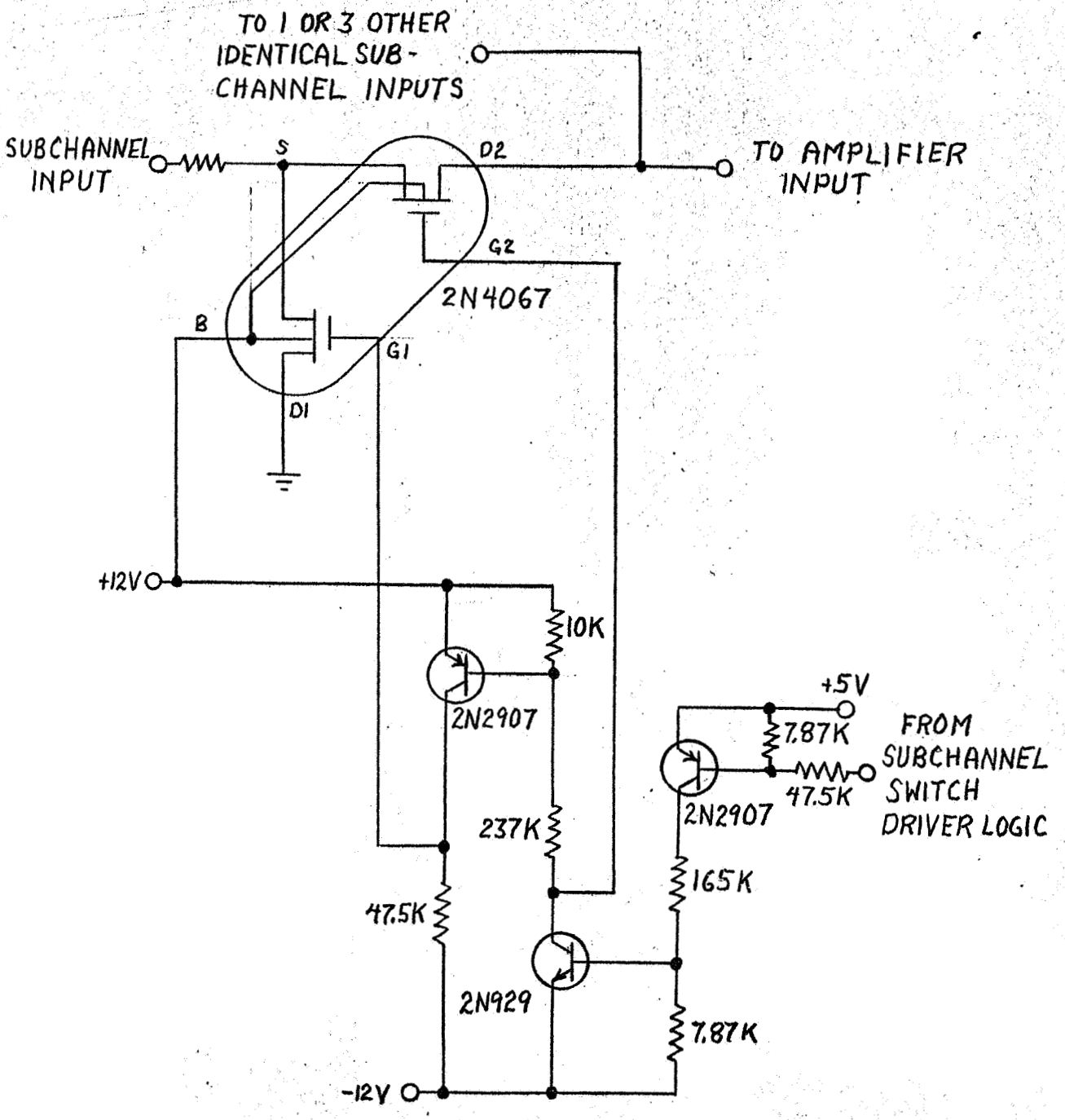


FIGURE II -11
MULTIPLEXER SWITCH AND DRIVER

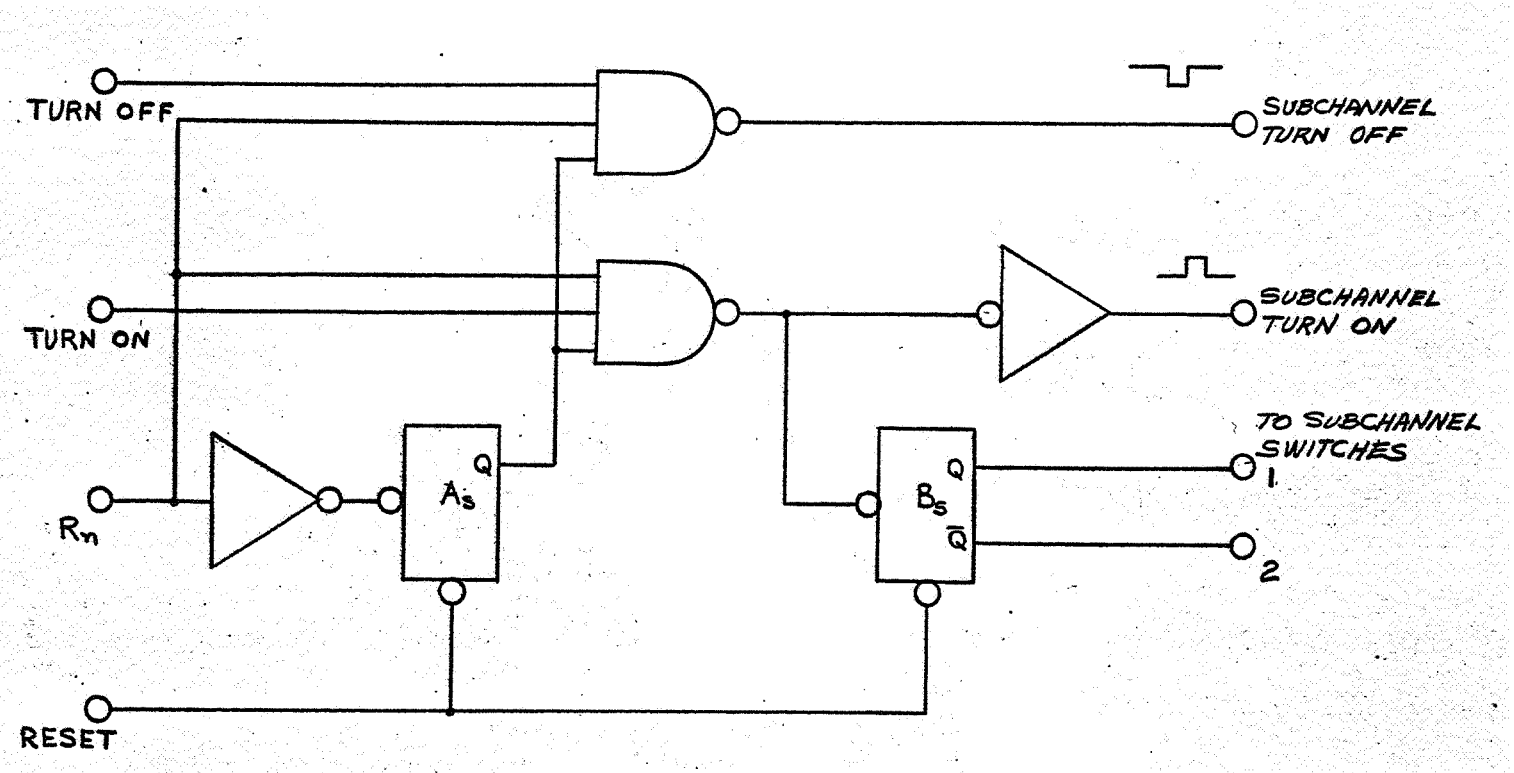


FIGURE II-12
TWO SUBCHANNEL SWITCH DRIVER

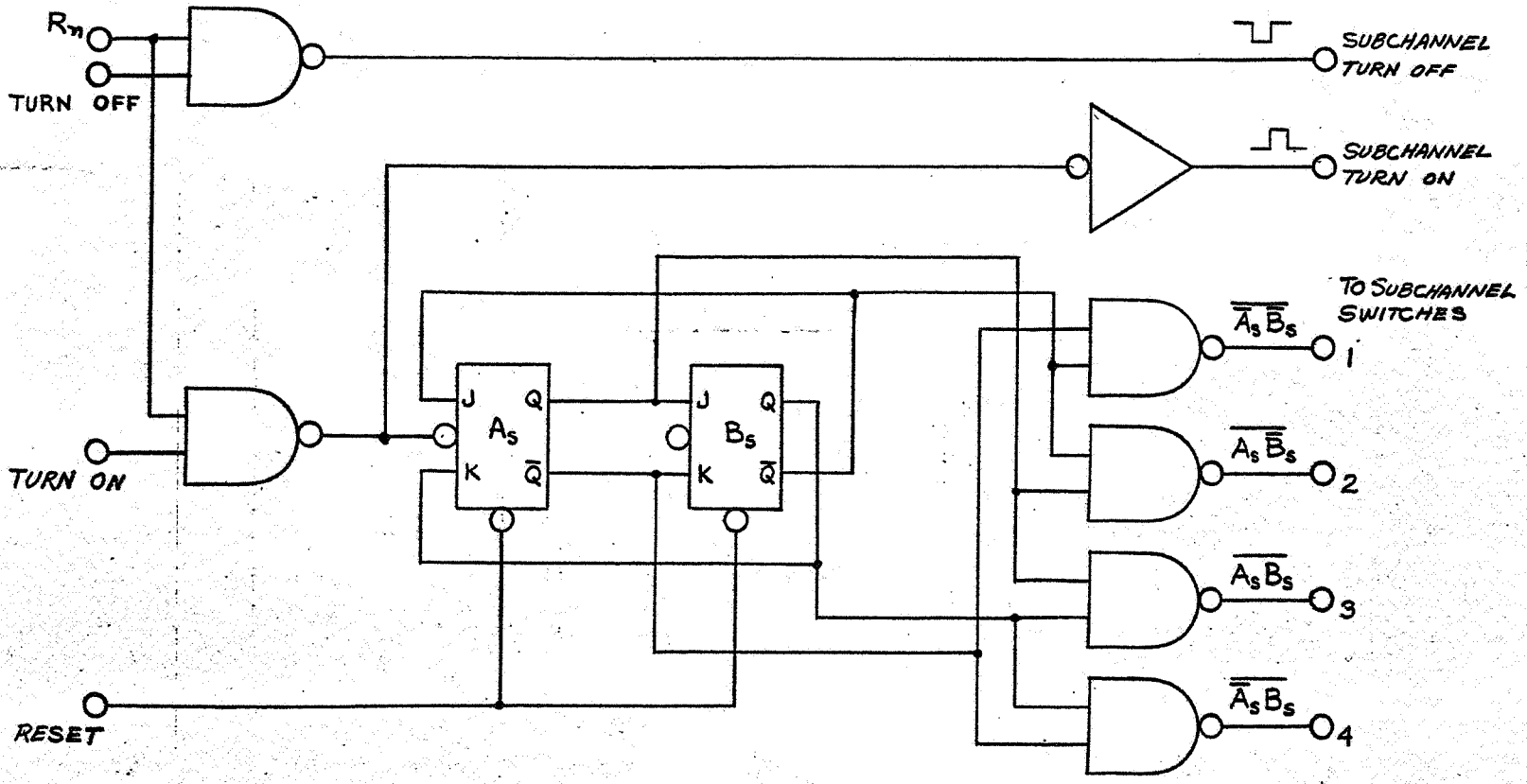


FIGURE II-13
FOUR SUBCHANNEL SWITCH DRIVER

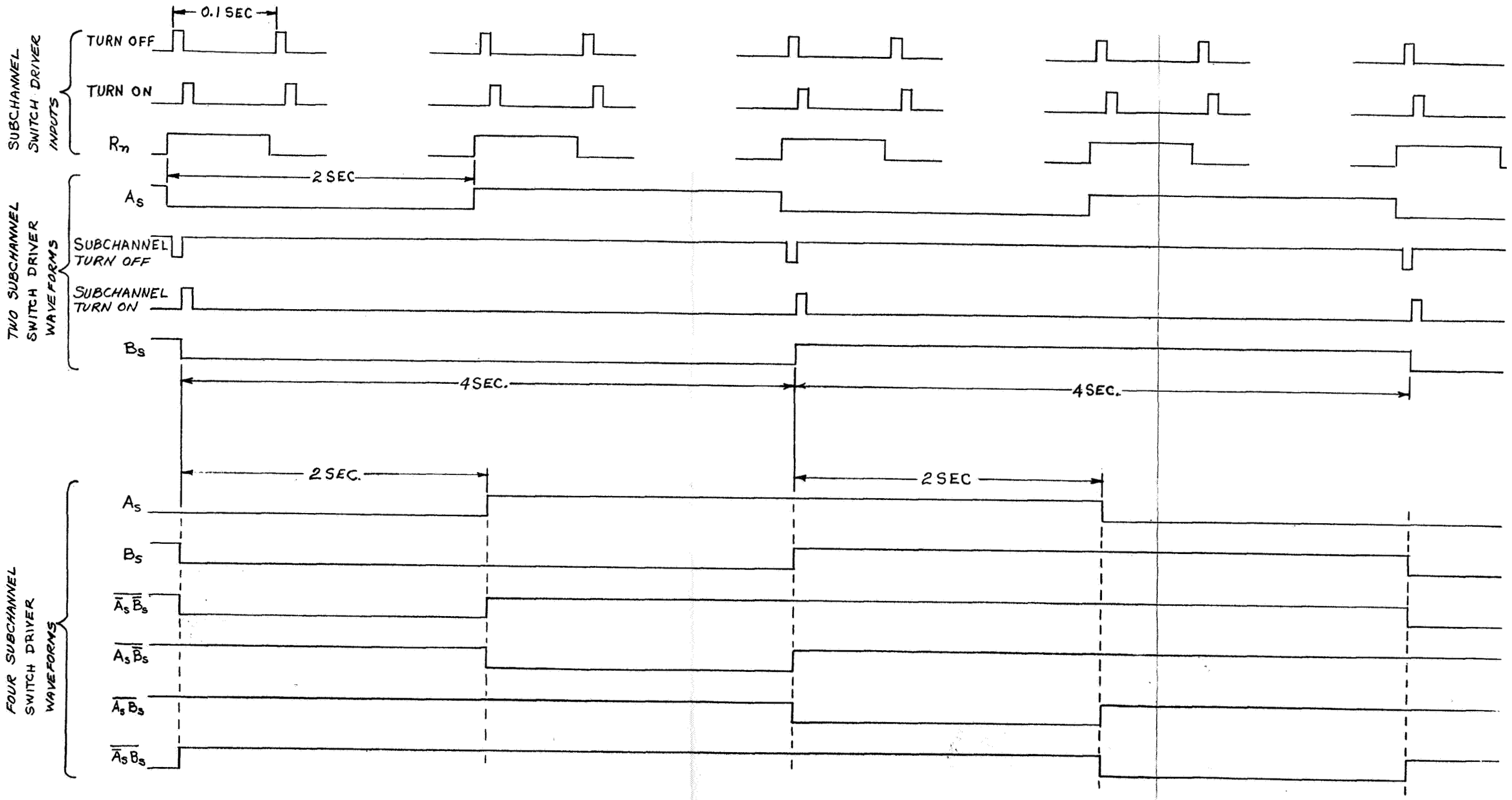


FIGURE II - 14
SUBCHANNEL SWITCH DRIVER WAVEFORMS

the amplifier from accidental shorts.

Figure II-15 shows a simplified circuit diagram of the amplifier. Also shown is the gain control circuitry which controls the turn off and turn on time of the signals. The important components are the amplifier A1, its gain determining resistors R1 and R2, the insulated gate field effect transistor (MOSFET) Q1, Capacitor C1, and bias resistors R4 and R5. Q1 is an enhancement mode MOSFET. Operation is as follows: Prior to TO, capacitor C1 is charged to -4.5 volts which biases Q1 close to but not in its conducting state. The reduce gain and restore gain control inputs are open so Q2 and Q3 are off. Since R1 and R2 are equal and Q1 is non-conducting the signal output equals the signal input - the gain is one. At TO the input to Q5 is grounded causing the NPN transistor Q3 to provide a constant charging current to capacitor C1. Thus the voltage across C1 gradually increases which gradually turns on Q1 to increase the feedback and reduce the gain. By T1, the resistance of Q1 is low enough to have reduced the gain to less than one-tenth. At T1, the input to Q5 goes positive and the input to Q4 also goes positive, turning Q3 off and Q2 on. Q2 provides a constant current discharge path for C1 and reverses the sequence. By T2, Q1 is again off and the original conditions are restored. R4 and R5 provide a reference point of approximately one-half the signal to avoid unequal starting points when the signal is positive or negative. This is necessary because the MOSFET is a unipolar device.

5. Channel Modules

The multiplexer channel circuitry is composed of the circuits discussed in Sections 3 and 4. Circuitry for two multiplexed channels, A and B, is on one plug-in board in the multiplexer layout. Thus twenty channels are on ten plug-in boards. The channel module plug-in boards use 3 of the possible combinations, a dual 1 channel plug-in, a dual 2 subchannel plug-in, and a dual 4 subchannel plug-in. These plug-ins are interchangeable and can be intermixed in any desired combination in the 10 positions provided. The sync code information required at the sync code "OR" gate inputs to generate the proper sync code is provided by the channel modules. Pin 1 of each channel module receptacle is connected to one of the 10 inputs of the 2's sync code OR gate. Pins 13 and 14 of each channel module receptacle are connected to one of the 20 inputs of the 4's sync code OR gate. The absence of a 2 or a 4 is used to indicate a single subchannel. In the following discussions of the channel modules the sync signal generation and distribution is discussed.

a. Dual One Channel Selector - The schematic for the dual one channel circuit is shown in Figure II-16. The module consists of only two channel amplifiers since the multiplexing switches and amplifier gain controls are not used. Since these are one channel switches no outputs to the sync code "OR" gates are required, thus the pins 1, 13 and 14 are connected to V_{cc} as unused inputs. The channel B half of the board has an R_{n+1} input which is inverted and routed to pin 15 as the sync to the next channel. This sync signal occurs in advance of the commutation time for the next channel by approximately 0.1 second or the time required to generate a complete sync word.

b. Dual Two Subchannel Selectors - The schematic for the dual two subchannel module is shown in Figure II-17. The circuits discussed in Sections 3 and 4 have been connected for the dual two subchannel systems. The sync input and the inverted R_n are ORed by the two sections of A3. This signal then feeds

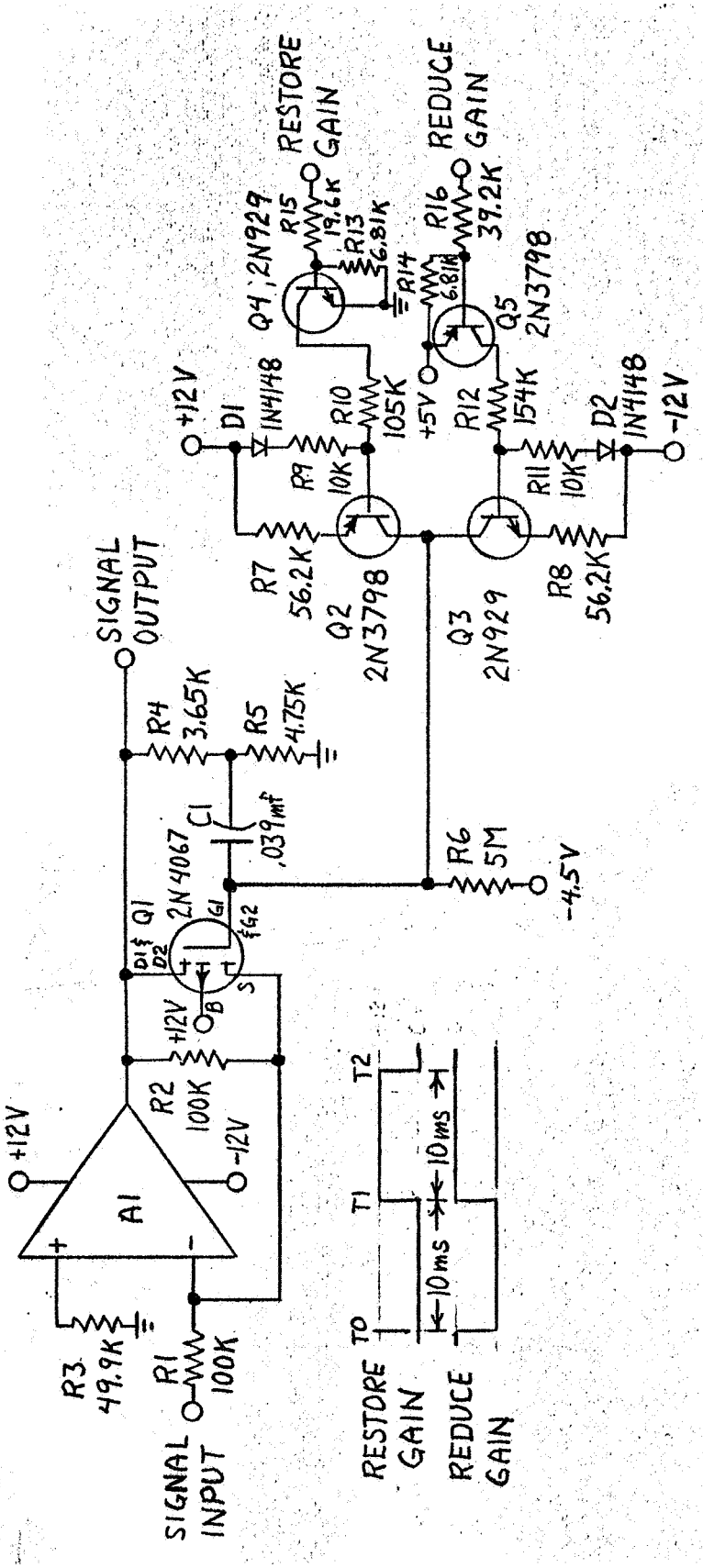
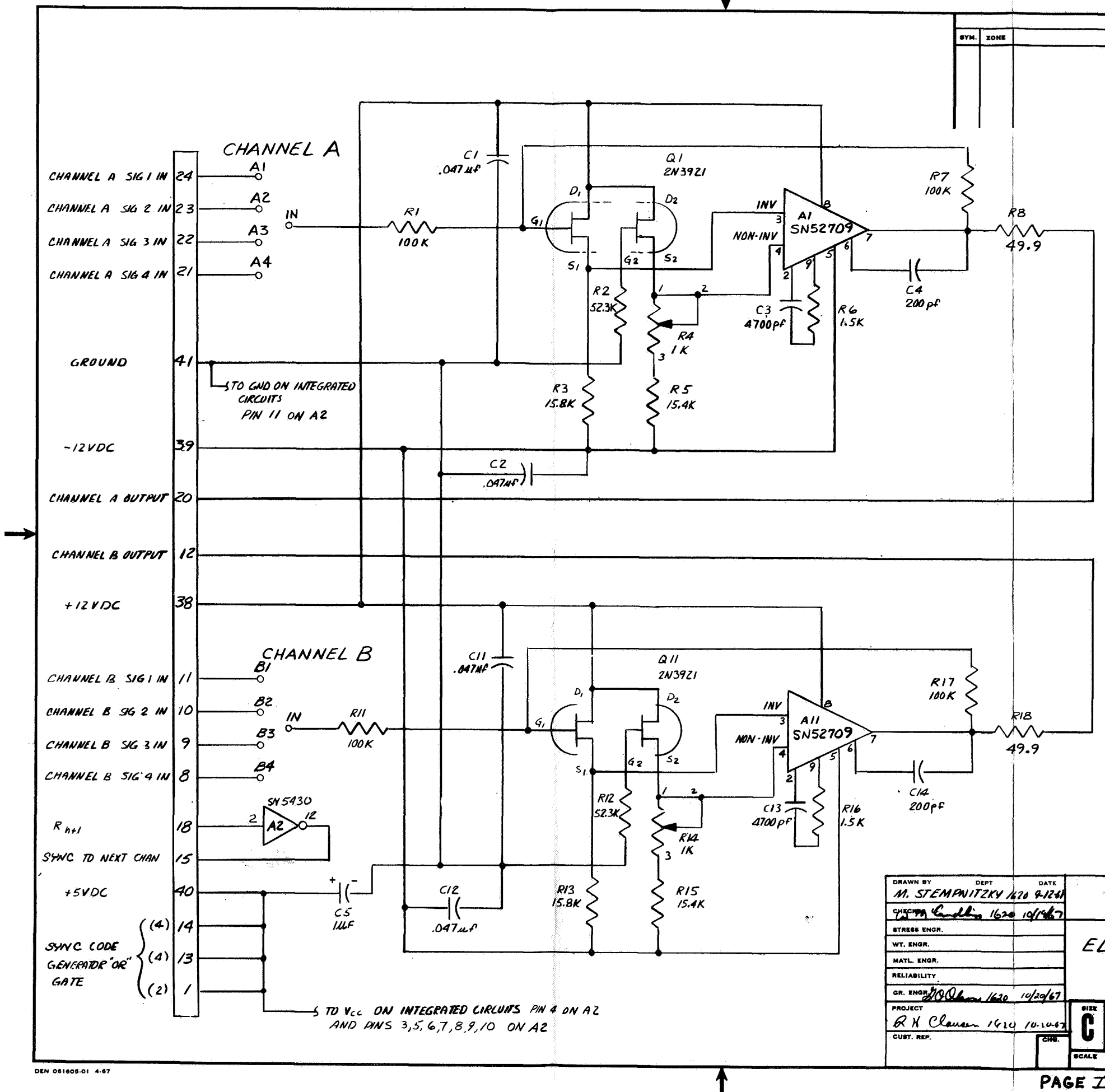


FIGURE II-15, MULTIPLEXER CHANNEL AMPLIFIER

REVISIONS				
SYM.	ZONE	DESCRIPTION	DATE	APPROVED



NOTES

1. REFERENCE DESIGNATIONS USED
   A1, A2, A11
   C1 - C5, C11 - C14
   Q1, Q11
   R1 - R8, R11 - R18
2. ALL RESISTANCE VALUES IN OHMS
3. REFERENCE DRAWINGS
   PRINTED WIRING ASSEMBLY
   21164-22
   PRINTED WIRING BOARD
   21164-32
   PRINTED WIRING MASTER
   21164-42

DRAWN BY	DEPT	DATE	MARTIN COMPANY
M. STEMPNITZKY	1620	9-12-67	DENVER, COLORADO
CHECKED	1620	10/19/67	ELECTRICAL SCHEMATIC
STRESS ENGR.			DUAL 1 CHANNEL SELECTOR
WT. ENGR.			
MATL. ENGR.			
RELIABILITY			
GR. ENGR.	1620	10/20/67	
PROJECT	1620	10-20-67	SIZE C · CODE IDENT. NO. 38597 · 21164-52
CUST. REP.			CHG. · SCALE · SHEET

DEN 081605-01 4-67

V_{cc} AND GROUND CHARACTERISTICS OF I.C.'s			
REF DESIGNATION	PART NO	PIN TERMINATED TO V_{cc}	PIN TERMINATED TO GROUND
A1	SN5473	3, 9, 7, 10, 14	11
A2	SN5410	1, 4, 14	11
A3	SN5410	6, 7, 8, 9, 10, 14	11
A4	SN5410	2, 4, 7, 8, 14	11
A5	SN5410	1, 2, 4, 7, 12, 14	11
A6	SN5473	3, 9, 7, 10, 14	11

CHANNEL A, OUTPUT 20
(4) SYNC CODE GEN OR GATE 14
+5 VDC 40
(3) SYNC CODE GEN OR GATE 13
CHANNEL A SIG 1 INPUT 24
CHANNEL A SIG 2 INPUT 23
CHANNEL A, SIG 3 INPUT 22
CHANNEL A, SIG 4 INPUT 21
(2) SYNC CODE GEN OR GATE 1
SYNC INPUT 16
R_{in} 19
TURN OFF 35
TURN ON 34
RESET 36
R_{in+1} 18
SYNC TO NEXT CHANNEL 15
CHANNEL B SIG 1 INPUT 11
CHANNEL B SIG 2 INPUT 10
CHANNEL B SIG 3 INPUT 9
CHANNEL B, SIG 4 INPUT 8
GND 41
+12 VDC 38
-12 VDC 39
CHANNEL B, OUTPUT 12
-4.5 VDC 37

SWITCH A A1
SWITCH A A2
SWITCH A A3
SWITCH A A4
1 SAS CHANNEL 1
2 SAS CHANNEL 2
SWITCH B B1
SWITCH B B2
SWITCH B B3
SWITCH B B4
1 SAS CHANNEL 1
2 SAS CHANNEL 2

→ TO V_{cc} ON INTEGRATED CIRCUITS
→ TO GND ON INTEGRATED CIRCUITS

SN5410/3 SN5410/3 SN5410/3 SN5410/3 SN5410/3 SN5410/3 SN5410/3 SN5410/3 SN5410/3 SN5410/3 SN5410/3 SN5410/3
SN 5473/2 SN 5473/2 SN 5473/2 SN 5473/2

CHANNEL A TURN OFF
CHANNEL A TURN ON
SAS CHANNEL SWITCH A-1 TURN ON
SAS CHANNEL SWITCH A-2 TURN ON
SAS CHANNEL SWITCH B-1 TURN ON
SAS CHANNEL SWITCH B-2 TURN ON
CHANNEL B TURN OFF
CHANNEL B TURN ON

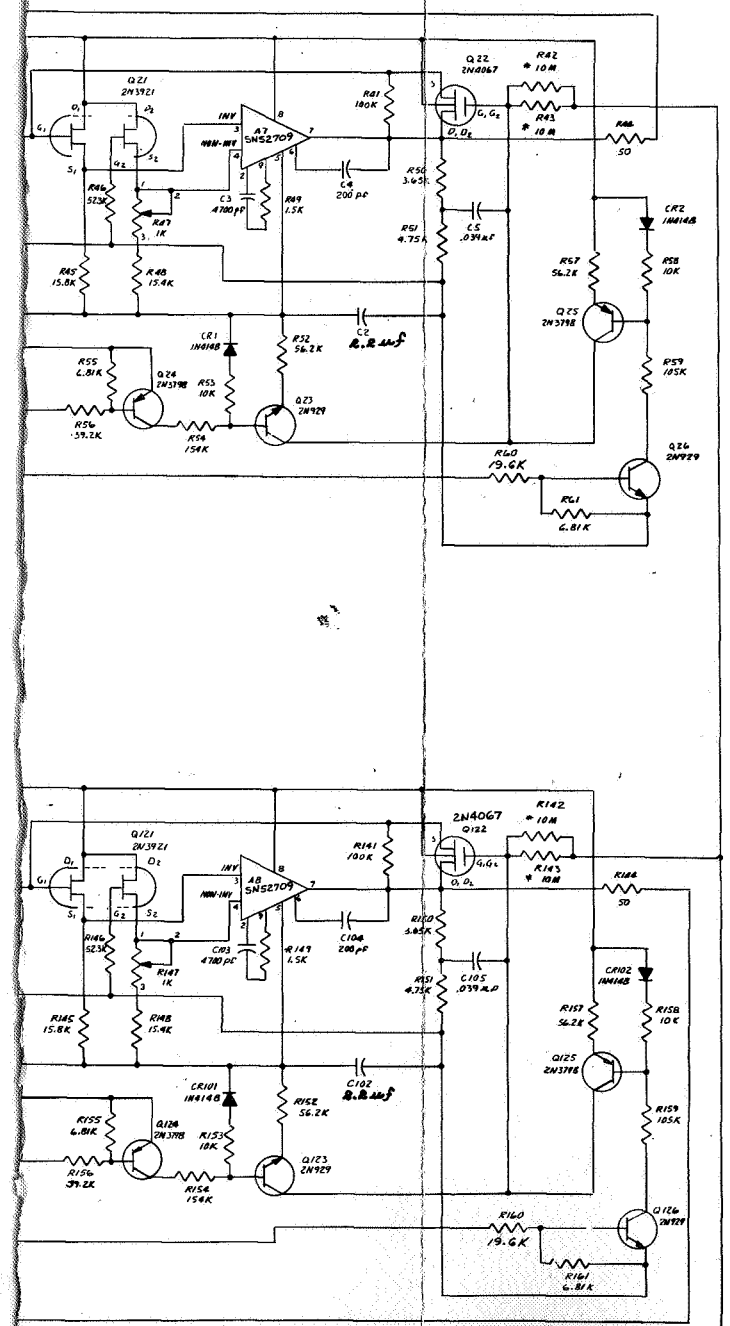
C6 1UF

Q7 2N2907 Q8 2N2907 Q9 2N929 Q10 2N4067
Q12 2N2907 Q13 2N2907 Q14 2N929 Q11 2N4067
Q15 2N2907 Q16 2N4067 Q17 2N2907 Q18 2N2907 Q19 2N929

Q1 2N4067 Q2 2N2907 Q3 2N2907 Q4 2N929
Q20 2N3921 Q21 2N3921 A7 SN52709 A8 SN52709
Q24 2N3798 Q23 2N929 Q122 2N3798 Q123 2N929
CR1 1N4148 CR100 1N4148
C1 .2.2 mf C101 .2.2 mf C102 .2.2 mf
C3 4700 pF C103 4700 pF C4 200 pF C104 200 pF
C5 4700 pF C105 4700 pF

2.

REVISIONS				
SYM	WHO	DESCRIPTION	DATE	APPROVED
A		R60 & R160 WERE 39.2K C1,2,101,102 WERE .047 μF	1/15/68	C.J.H.



REFERENCE DESIGNATIONS USED

1. A1 - A8

   Q1 - Q4, Q6 - Q9, Q11 - Q14, Q16 - Q19, Q21 - Q24, Q121 - Q126.

   R1 - R8, R11 - R18, R21 - R28, R31 - R38, R41 - R51, R141 - R161.

   C1 - C5, C4
   C101 - C105

   CR1 - CR2
   CR101 - CR102

2. REFERENCE DRAWINGS
   PRINTED WIRING ASSEMBLY 21164-23
   PRINTED WIRING BOARD 21164-33
   PRINTED WIRING MASTER 21164-43

3. ALL RESISTANCE VALUES IN OHMS. ALL RESISTORS 1% EXCEPT as ± 5%

PAGE II-22 FIGURE II-17

STEMPHITERY 1620 9-17-67	MARTIN COMPANY DENVER, COLORADO	
	ELECTRICAL SCHEMATIC DUAL 2 SUBCHANNEL SWITCH	
CTOL IDENT NO 30507	SIZE J	21164-53
SCALE	SHEET	

one of the inputs to the 2's OR gate via pin 1. The channel B half of the board has an R_{n+1} input which is inverted and routed to pin 15 as the sync to the next channel as discussed in the one channel case. Pins 13 and 14 are tied to V_{cc} as unused inputs to the 4's sync code OR gate.

c. Dual Four Subchannel Selectors - The schematic for the dual four subchannel module is shown in Figure II-18. The circuits discussed in Sections 3 and 4 have been connected for the dual four subchannel systems. The channel A and B turn off signals are in the proper time position to be used for sync signals. Thus the channel A turn off signal is the sync for channel B and the sync for channel A is fed thru from the previous channel. The channel B turn off signal is the sync signal for the succeeding channels. Pin 1 is tied to V_{cc} as an unused input of the 2's sync code OR gate.

6. Power Supply

The power supply shown by the schematic diagram, Figure No. II-19, consists of a switching series pre-regulator, a dc to dc converter and secondary rectifiers and filters.

Transistors Q2 and Q3 are the switching regulators and are controlled by transistors Q1, Q4, and Q5 and the associated circuits. Operation is as follows: With no voltage across C3, Q1 is saturated by bias resistor R1 and in turn Q2 and Q3 are saturated. C3 is thus charged through L2. When the voltage of C3 is great enough to exceed the reverse bias voltage of Q5 (provided by CR5), Q4 and Q1 saturate. The saturation of Q1 "grounds" R1 through Diode CR3 and turns off Q3, Q2 and Q1. These transistors remain turned off while C3 discharges into the load until C3 voltage is reduced below the threshold of Q5. At this point Q3, Q2 and Q1 are turned on and the cycle repeated. The combination of L3 and C3 is selected to give the circuit some hysteresis for proper operation. In the case shown here the threshold of Q5 is set to charge C3 to approximately 20 volts.

If the input voltage is raised the intervals of current flow are reduced in duration. Reduction in load will have the same effect. Consequently the voltage C3 is held about constant.

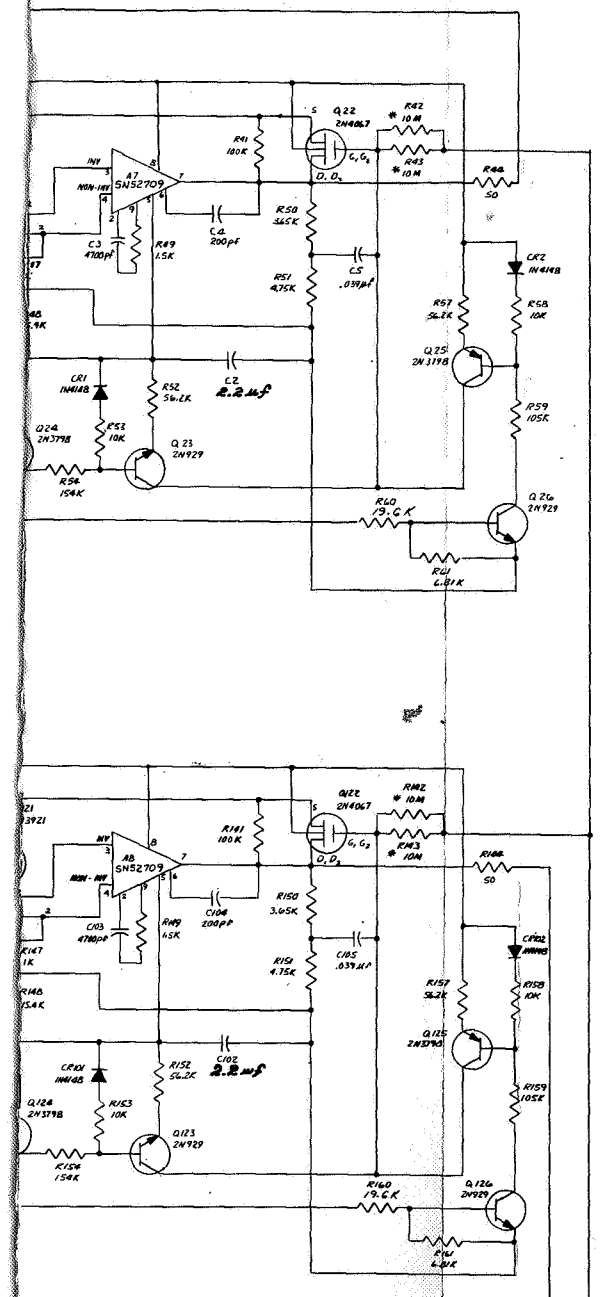
In the design shown C1, C2 and L1 form an LC pi network to reduce RFI problems. CR1 prevents the application of damaging reverse voltage to the circuit. L3 and C4 form a decoupling network to reduce interaction between the pre-regulator and the converter.

The dc to dc converter is quite conventional. Operation is based upon saturation of a square-loop core in alternate directions. The frequency of oscillation is approximately 5 KC. Transistors Q6 and Q7 perform switching of current through alternate halves of the winding and R12 provides starting bias for the transistors. CR6 and R16 complete the base-emitter drive current path and C10 speeds up switching. Q6 and Q7 are selected for low saturation voltage, good speed, adequate current rating and a voltage (V_{CE}) rating of greater than twice the collector voltage. C5 and R11 reduce switching spikes.

CHANNEL A, 5Hz 1 IN
CHANNEL A, 5Hz 3 IN
CHANNEL B, 5Hz 1 IN
CHANNEL B, 5Hz 3 IN
CHANNEL B, 5Hz 2 IN
(4)SYNC CHECK OR GATE
R A
TURN OFF
CHANNEL A ARMED
(2)SYNC CHECK OR GATE
+5VDC
GND
+12VDC
-12VDC
CHANNEL A, 5Hz 2 IN
SYNC TO MAST CHANNEL
MAST
R A11
SYNC INPUT
5 SYNC CHCK CANCELLATION "OR" GATES (4)
TURN ON
CHANNEL A, 5Hz 4 IN
CHANNEL B, 5Hz 4 IN
+5VDC
(2)SYNC CHECK OR GATE
CHANNEL B, OUTPUT
-4.5VDC

2

REVISIONS				
PRS	ZONE		DATE	APPROVED
A		R109 R160 WERE 39.2 K C1,2,101,102 WERE .047 μf	1/5/8	CW4L



NOTES

1. REFERENCE DESIGNATIONS USED

   A1 - A8

   Q1 - Q4 , Q6 - Q9 , Q11 - Q14 , Q16 - Q19 , Q21 - Q24
   Q101 - Q104 , Q106 - Q109 , Q111 - Q114 , Q116 - Q119 , Q121 - Q126

   R1 - R8 , R11 - R18 , R21 - R28 , R31 - R38 , R41 - E61
   R101 - R108 , R111 - R118 , R121 - R128 , R131 - R138 , R141 - R161

   C1 - C5 , C6
   C101 - C106

   CR1 - CR2
   CR101 - CR102

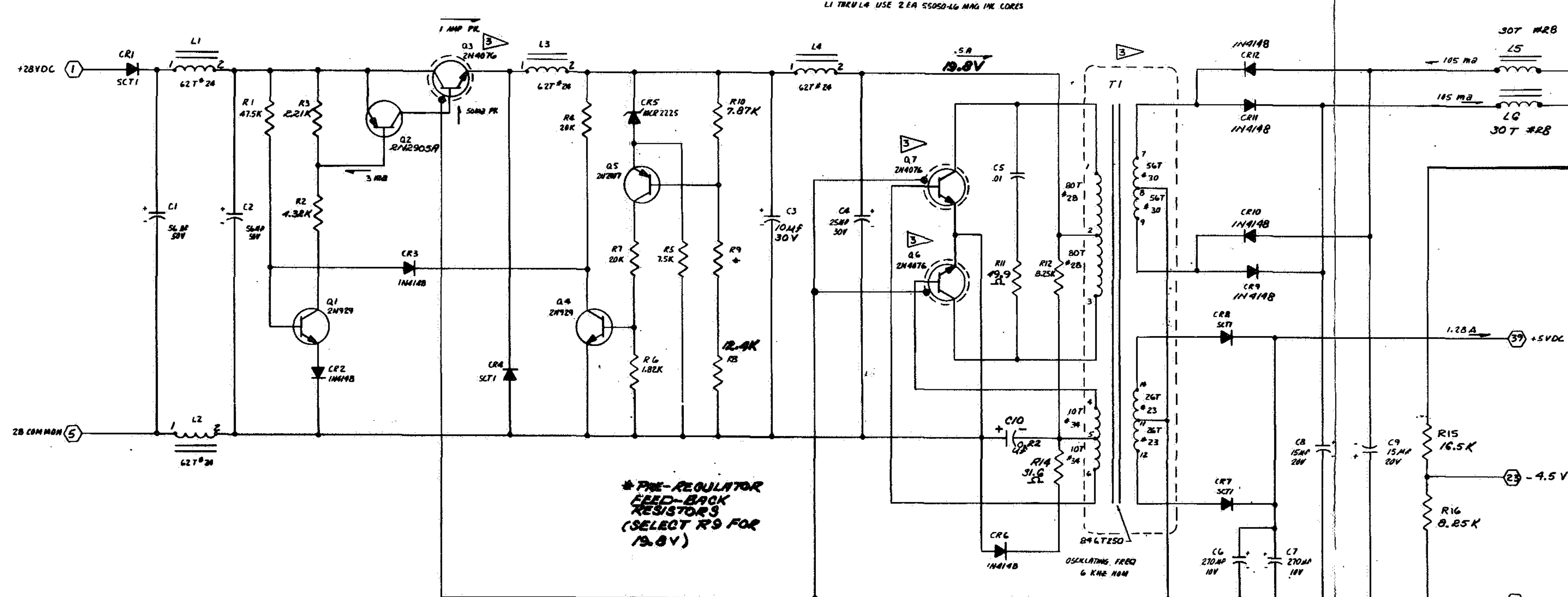
2. ALL RESISTANCE VALUES IN OHMS. ALL RESISTORS 1% EXCEPT * = 5%.
3. REFERENCE DRAWINGS
   PRINTED WIRING ASSEMBLY 21164-24
   FABRITED WIRING BOARD 21164-34
   PRINTED WIRING MASTER 21164-44

PINS CONNECTED TO Vcc		PINS CONNECTED TO GROUND	
FUNCTIONAL DESIGNATIONS	PIN NUMBER	PIN NUMBER	TYPE
A1	4	11	SN5400
A2	4	11	SN5473
A3	4,10,12	11	SN5400
A4	4,10,12,13	11	SN5400
A5	4	11	SN5473
A6	4	11	SN5400

PAGE II-24 FIGURE II-18

DRAWN BY STEMPNITZKY 4120 2-7-68	MARTIN COMPANY DENVER COLO.	
CHECKED BY Van Allen 4-24 4-17-68	ELECTRICAL SCHEMATIC DUAL 4 SUBCHANNEL SWITCH	
STRESS ENGR		
MT. ENGR		
MATL. TABS		
RELIABILITY		
QA PROJ.		
PROJECT A.H. CEA Van Allen 4-24 4-17-68	CODE IDENT NO 38987	SIZE J / 21164-54
DWG NO	SCALE NONE	SHEET 1 OF 1

SYM.	ZONE	DESCRIPTION	DATE	APPROVED
A		REVISED CIRCUITRY. REVISE VALUES OF R2, R3, R8, R10, R11, R14, R15, R16, CR9-CR12, C3. REMOVED R13. ADDED L5, L6.	1/19/8	



NOTES

1. ALL RESISTANCE VALUES IN OHMS
2. HIGHEST REFERANCE DESIGNATIONS USED R16, C10, CR12, T1, L6 & Q7 NOT USED R13
3. Q3, Q6, Q7 CASES AND T1 SHIELD TIE TO SIGNAL GROUND AS SHOWN.
4. REFERENCE DRAWINGS
   PRINTED WIRING ASSEMBLY 21164-28
   PRINTED WIRING BOARD 21164-38
   PRINTED WIRING MASTER 21164-48

MARTIN MARIETTA CORPORATION
DENVER DIVISION P.O. BOX 179
DENVER, COLORADO

ELECTRICAL SCHEMATIC
POWER SUPPLY

E 38597 21164-58

PAGE II-25 FIGURE II-19

21164-58

All secondar rectification and filtering is conventional. All filtering is capacitive input and has been found adequate. Secondary regulation is not employed on the secondary windings since better than 3% regulation is obtained without further regulation.

7. Interconnections

Figure II-20 shows the interconnections in the multiplexer. All interconnection between plug-in modules are made by a printed circuit mother board. All interconnections between the mother board and the power input, signal inputs and signal output connectors are made by printed cables. Interconnection from the connectors to the case are made by wires.

1

2

CHASSIS GROUND
+28 V
+28V RETURN
J18
C1
C2
J14
A14
POWER SUPPLY
GROUND
+5 VDC
+12 VDC
-4.5 VDC
-12 VDC
CHANNEL 11
CHANNEL 13
CHANNEL 15
CHANNEL 17
CHANNEL 19
J6
J7
J8
J9
J10
A6
A7
A8
A9
A10
CHANNEL A
CHANNEL B
CHANNEL 11 OUTPUT
CHANNEL 18 OUTPUT
CHANNEL 19 OUTPUT
CHANNEL 20 OUTPUT
SYNC CODE OUTPUT
J17
A13
SYNC CODE GENERATOR - "OR" - GATES
A12
SYNC CODE GEN.
J13
J12
J15
J16
CHANNEL 12
CHANNEL 14
CHANNEL 16
CHANNEL 18
CHANNEL 20
CHANNEL 10
CHANNEL 8
CHANNEL 6
CHANNEL 4
CHANNEL 2
GROUND SIGNAL SHIELD
CHASSIS GROUND
CHANNEL 9
CHANNEL 7
CHANNEL 5
CHANNEL 3
CHANNEL 1
A5
A4
A3
A2
A1
J5
J4
J3
J2
J1
A11
SEQUENCE GENERATOR
J11
SYNC INVERT COMMAND
SYNC TRANSFER
TURN ON
TURN OFF
RESET
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
R17
R18
R19
R20
CHANNEL 2 OUTPUT
CHANNEL 1 OUTPUT
GROUND-SIGNAL SHIELD
CHASSIS GROUND
CHANNEL 4 OUTPUT
CHANNEL 3 OUTPUT

2

REVISIONS				
LTR	DESCRIPTION	DATE	APPROVED
A	ADD (2) .047 μF CAPACITORS #26 & #28 TO J18 (C1 & C2)	4/26	C.Hall

J17

P1 CHANNEL 11 OUTPUT
12
13
14
15
16
17
P18 CHANNEL 18 OUTPUT

P19 CHANNEL 19 OUTPUT

P20 CHANNEL 20 OUTPUT

P21 SYNC CODE OUTPUT

J17

P2 CHANNEL 2 OUTPUT

P3 CHANNEL 1 OUTPUT

P4 GROUND-SIGNAL SHIELD

P5 CHASSIS GROUND

P6 CHANNEL 4 OUTPUT
3
8
5
8
7
10
P9 CHANNEL 9 OUTPUT

NOTE

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER AND ASSEMBLY DESIGNATION PER MSFC-STD-349.

2. REFERENCE DRAWINGS—

21164-52	ELECTRICAL SCHEMATIC	A1-A5
21164-53		A6-A8
21164-54		A9-A10
21164-55		A11
21164-56		A12
21164-57		A13
21164-58	ELECTRICAL SCHEMATIC	A14

21164-21 PRINTED WIRING ASSEMBLY
21164-1 MULTIPLEXER A334

DRAWN	C. Hall	1620	1-24-8
CHECKED			
STRESS ENGR.			
MT. ENGR.			
MFG. ENGR.			
RELIABILITY			
ME ENGR.			
PROJECT			
CONT. REQ.			

MARTIN MARIETTA CORPORATION
DENVER DIVISION P.O. BOX 179
DENVER, COLORADO

SCHEMATIC -
AUXILIARY TIME DIV.
MULTIPLEXER ASSY.

SIZE	CODE IDENT NO	
J	04236	21164-2
SCALE NONE		SHEET

C. DEMULTIPLEXER

The SSB/DSB auxiliary time division demultiplexer block diagram is shown in Figure II-21. Most of the circuitry is used to synchronize the demultiplexing. The clock is regenerated using the level transition that always occurs at the middle of each bit. This clock is used to demodulate the sync code and shift it serially into a 20 stage register. Since the sync code is comma free, the sync word decoder continuously monitors the register for any of the six code words. The decoder has four outputs, three of which indicate, for each channel in sequence, whether the channel is multiplexed with 1, 2 or 4 subchannels. The fourth output is a reset pulse generated by reception of one of the three complemented code words every 8 seconds. Sequence regeneration is accomplished by a 20 stage ring counter that is reset by the reset pulse. The three channel selector switches select one of the twenty channel inputs and the corresponding ring counter stage output. The subchannel decoder uses the ring counter information to extract the demultiplexing data, i.e., 1, 2 or 4 subchannels, from the sync word decoder outputs. The reset pulse provides cycle synchronization for subchannel identification. The demultiplexing switches are two DPDT relays per channel whose position is determined by the channel decoder outputs and the channel selected. The channel decoder outputs and the channel selected are also used to generate the subchannel sync outputs that indicate an active subchannel by a positive output. An error signal is generated in the ring counter when a 1, 2 or 4 sync word is not received every 20 clock pulses. The error pulse advances the ring counter to minimize the effect of a sync code error.

1. Clock Regeneration

The circuitry for clock regeneration is shown in Figure II-22 along with the sync code demodulator and the first four stages of the 20 stage shift register and the 1st level decoder for them. Clock regeneration depends on the level transition that always occurs in the middle of each sync code bit. In Figure II-22, two single-shot multivibrators, A12 and A11, detect the negative going and positive going transitions respectively. Each produces a 10 micro sec. pulse. Either of these pulses can trigger single-shot A5 if single-shot A1 is not in its active state. Single-shot A1 is triggered by the trailing edge of pulse generated by A5. Both A5 and A1 produce pulses of approximately 1.875 milliseconds. This timing results in blocking the input to A5 for the period from 1.88 to 3.75 milliseconds after it has been triggered. The sync code input produces a series of pulses from A11 and A12 every 5 milliseconds due to the level transition that always occurs in the middle of each bit. However, the sync code input will produce a pulse midway between these only when two similar bits occur in sequence in the sync code word. Thus, if the clock regeneration circuit starts on the pulses that do not occur every 5 milliseconds, it will slip to the proper phase the first time a pulse is missing and will then remain locked with the pulses that do occur every 5 milliseconds. These pulses are used through appropriate drivers as the shift pulses for the sync code register. The waveforms generated by these circuits are shown in Figure II-23.

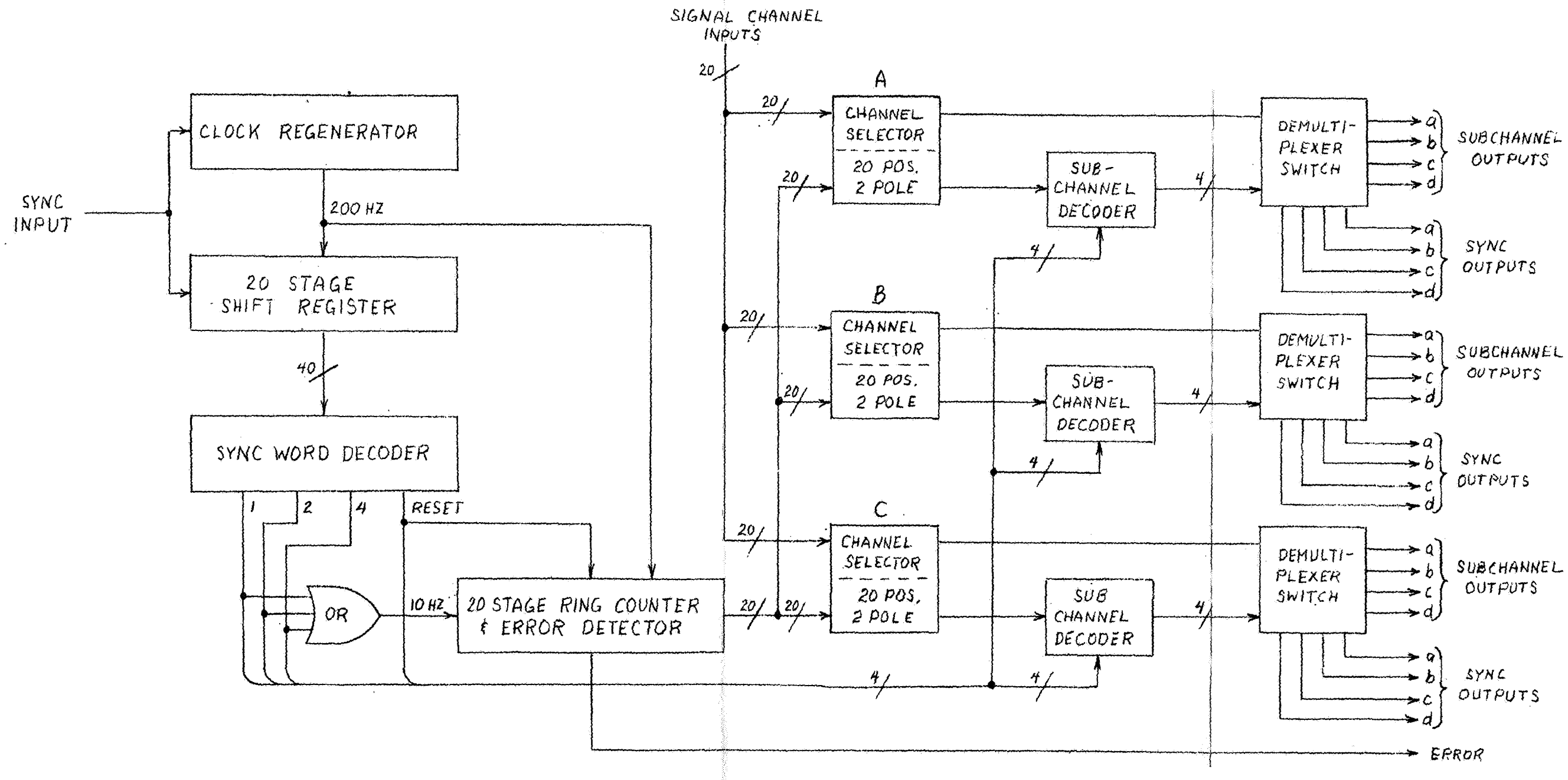
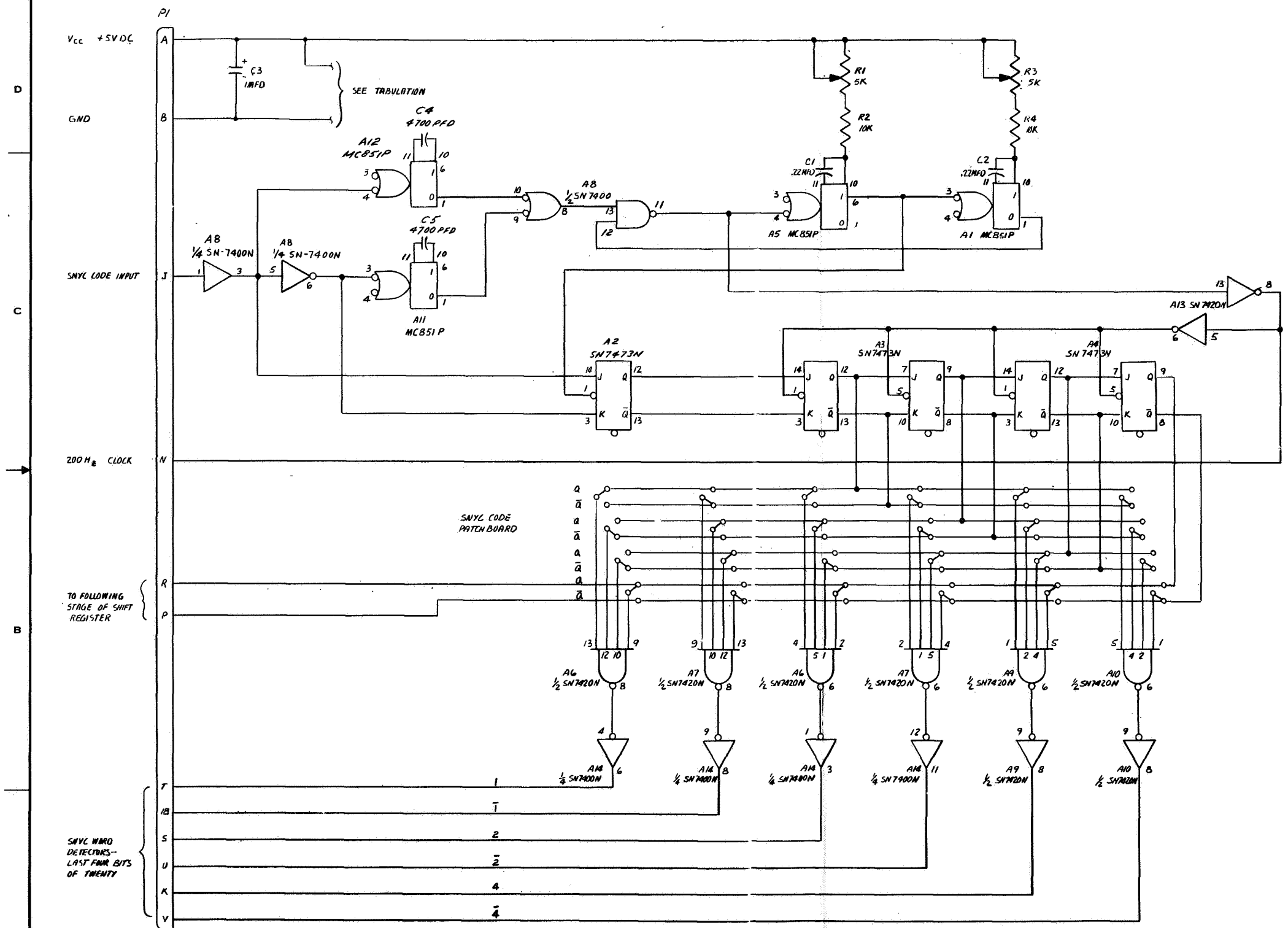


FIGURE II-21
DEMULTIPLEXER BLOCK DIAGRAM

REVISIONS				
SYM.	ZONE	DESCRIPTION	DATE	APPROVED
A		ADDED C4 & C5, A8 WAS SN7410N & GENERAL REVISIONS	1-29-68 WRM	



REF DESIG	PIN CONNECTED TO V_{cc}	PIN CONNECTED TO GND
A1	14, 4	7
A3, A4	2, 9, 6	11
A5	14, 3	7
A6, A7	14	7
A8	14, 4, 2	7
A9, A10	10, 12, 13, 14	7
A13	1, 2, 4, 9, 10, 12, 13	7
A14	2, 5, 10, 13, 14	7
A11	14, 4, 9	7
A12	14, 3, 9	7
A2	2, 4	11

DRAWN BY STEMPNITZKY	DEPT. 1620	DATE 11-9-67	MARTIN MARIETTA CORPORATION
CHECKER		11-15-67	DENVER DIVISION P.O. BOX 179 DENVER, COLORADO
STRESS ENGR.			SNYC CODE SHIFT REGISTER AND CLOCK REGENERATOR DEMULTIPLEXER
WT. ENGR.			
MATL. ENGR.			
RELIABILITY			
GR. ENGR.		1620 1/30/68	SIZE D CODE IDENT. NO. 04236 21164-121
PROJECT			SCALE NONE SHEET 1
CUST. REP.		1620 1/30/68	SIZE A

DEN 081807-01 10-001

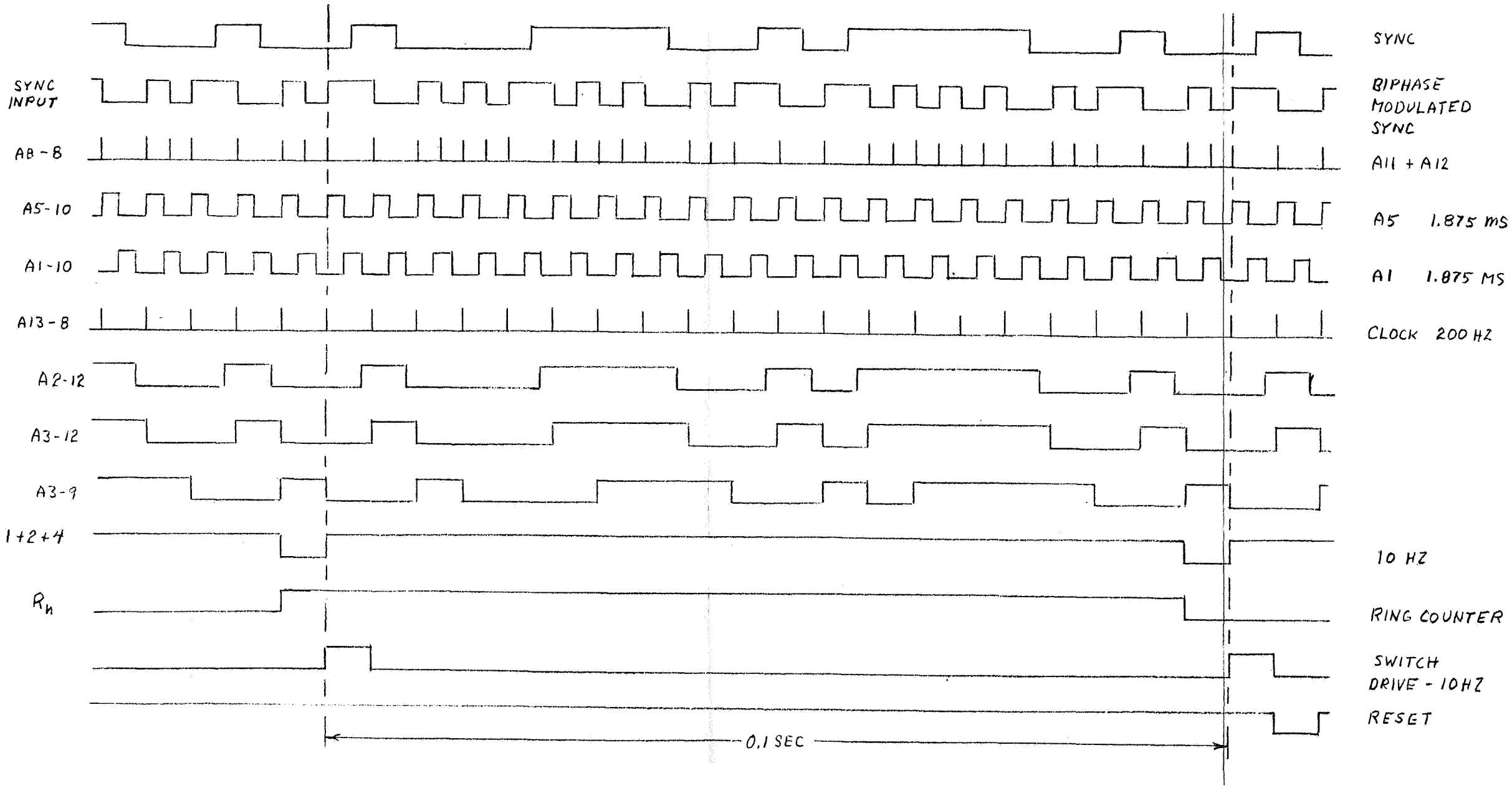


FIGURE II-23
DEMULTIPLEXER SYNC WAVEFORMS

2. Synchronization

a. Demodulation of Sync Code - The demodulation of the sync code, i.e., removing the 400 Hz component, is accomplished by using the output of single-shot A5 to shift the sync code into flip-flop A2 at the trailing edge of the pulse produced by A5.

b. Sync Code Shift Register - The 20 stage sync code shift register is a straightforward shift register that uses the regenerated 200 Hz clock to shift the sync code serially into the register. It is located on three different plug-in boards to alleviate a connector pin limitation. 4 stages are on the same board as the clock regeneration circuits, Figure II-22, and the remaining 16 stages are on two boards of 8 stages each, Figures II-24, and II-25, each of these boards have clock drivers.

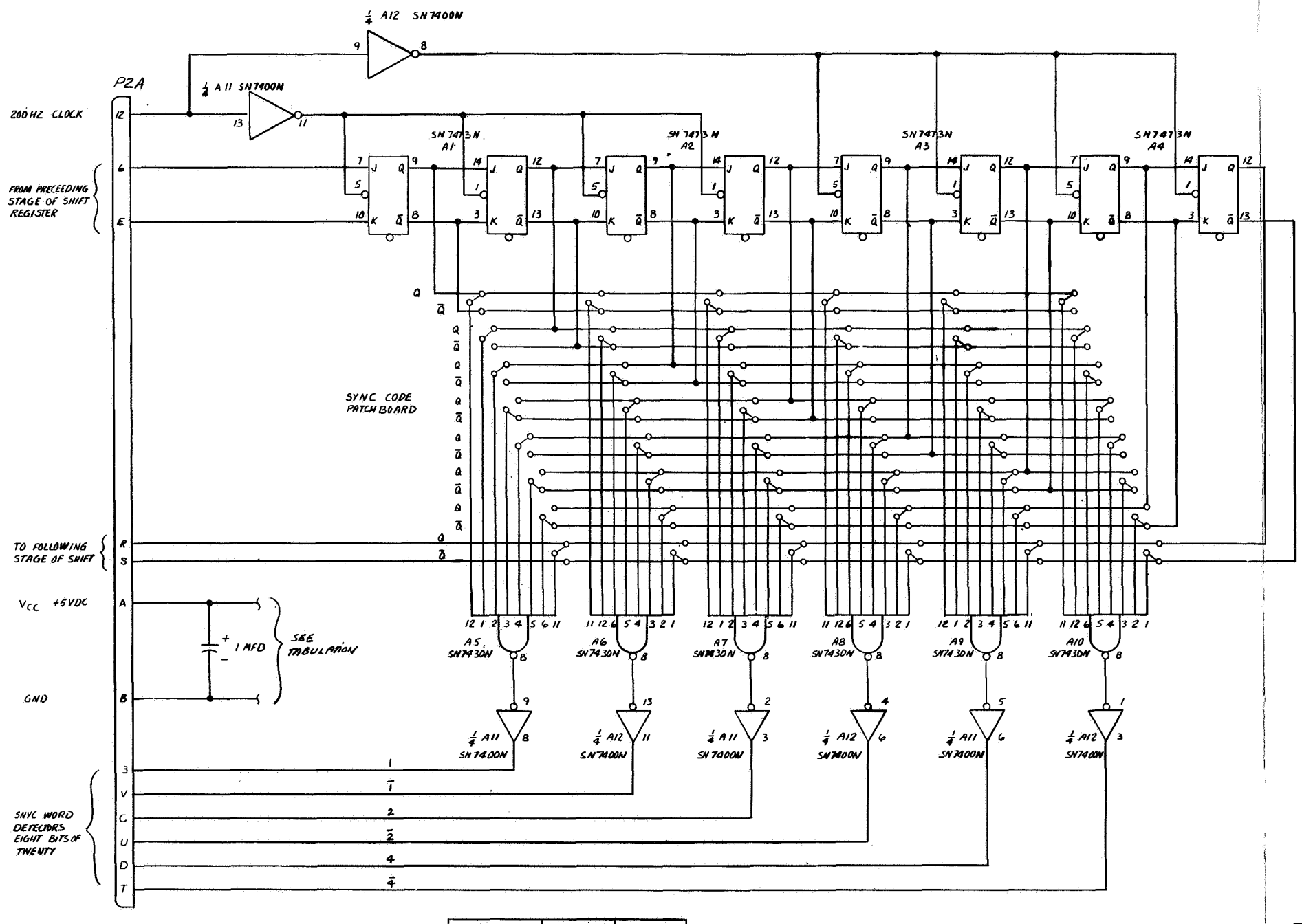
c. Sync Code Word Detector - The sync code word detector is also divided to avoid pin limitation problems. 4 bits are decoded on the same board as the clock regeneration, Figure II-22, and 8 bits are decoded on each of the two shift register boards, Figures II-24 and II-25. These partially decoded outputs are then combined on the decoder board, Figure II-26, to complete the decoding with the six 3-input AND gates. These six outputs correspond to the six code words -- one each for a single subchannel channel, a 2 subchannel channel, a 4 subchannel channel, and the three complements of these for channel 1 at the beginning of each cycle. Sync word decoding is hardwired programable to decode the sync codes selected for the multiplexer.

d. Sequence Regeneration - Sequence regeneration is performed by a 20 stage ring counter, Figure II-27, that advances one state with each detected sync word (1, 2 or 4) from the OR gate shown in Figure II-26. This produces a sequence of 20 R_n pulses, R1 through R20, that are synchronous with the channel switching times. These are connected to one deck of the rotary selector switches. Cycle synchronization is accomplished by the detection of one of the complements. This reset pulse is delayed 2 clock pulses or 10 milliseconds by the circuitry shown in Figure II-26 to ensure that no switching spikes can occur. The demultiplexer switch drive shown on Figure II-27 is also delayed 1 clock pulse or 5 milliseconds to avoid switching spikes.

e. Error Detection - The error detection circuitry is shown in Figure II-27 and consists of 5 flip-flops, a 4 input AND gate and drivers as required. The 5 flip-flops are connected as a binary counter and are driven by the 200 Hz detected clock. The 4 input AND gate is connected to detect the 22nd and 23rd clock pulses thus producing a 10 millisecond error pulse. However, this pulse is not produced if a 1, 2 or 4 code is detected because a detected 1, 2 or 4 code resets the counter to zero every 20 bits. If only one code word is missed, the ring counter does not lose synchronization because the error signal is used to advance the ring counter.

If repetitive code words are missed the error signal repeats every 32 clock pulses or every 160 milliseconds. This is an indication that the proper synchronization code words are not occurring even though a clock signal has been regenerated.

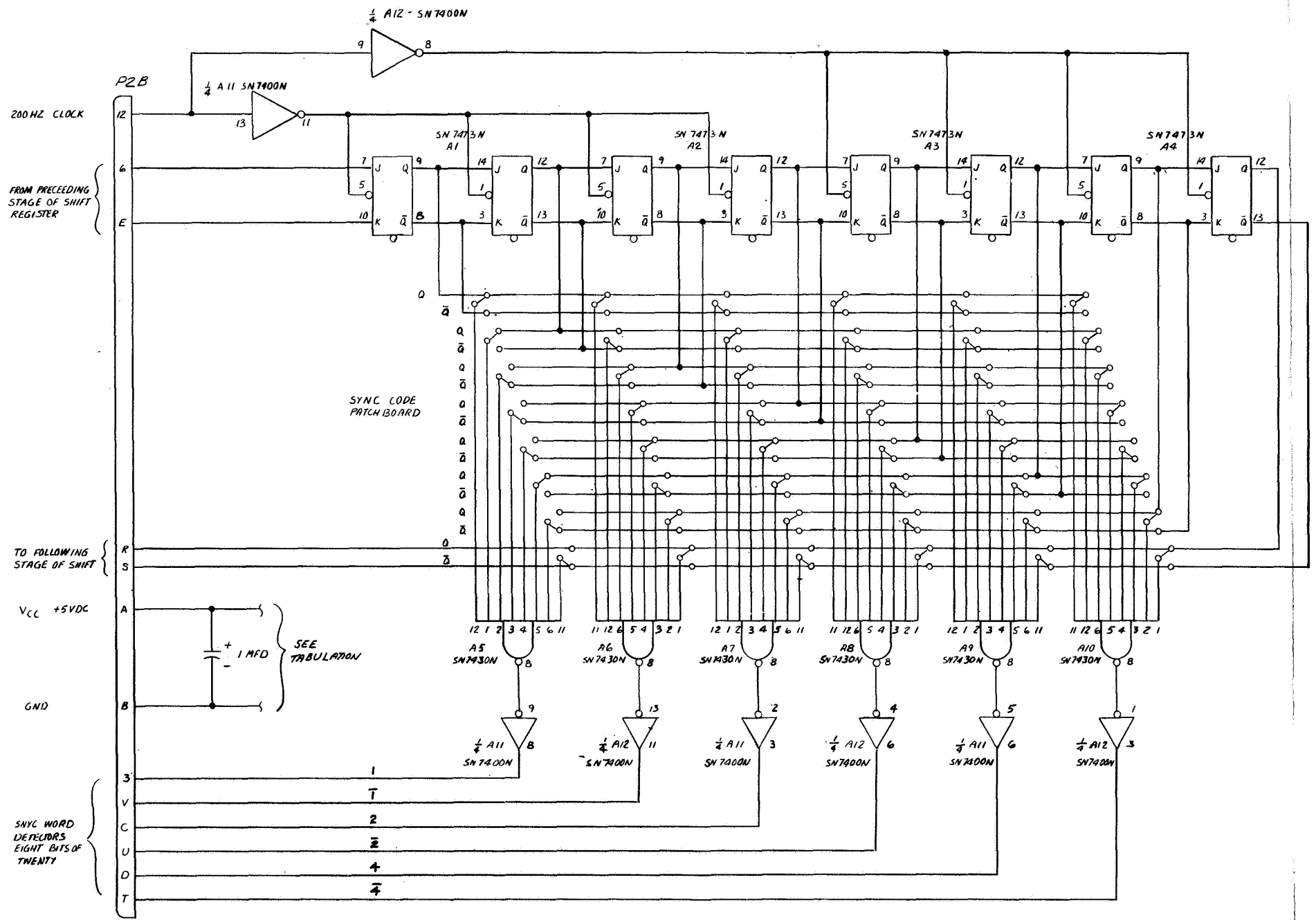
REVISIONS				
SYM.	ZONE	DESCRIPTION	DATE	APPROVED



REF DESIG	V_{CC} CONN	GND CONN
A1 THRU A4	2 4 6	11
A5 THRU A10	14	7
A11	1,4,10,12,14	7
A12	2,5,10,12,14	7

DRAWN BY	DEPT.	DATE	MARTIN MARIETTA CORPORATION
STEMPNITZKY	1620	11-9-67	DENVER DIVISION P.O. BOX 179 DENVER, COLORADO
CHECKER		11-14-67	
STRESS ENGR.			SYNC CODE SHIFT REGISTER AND DECODER #1
WT. ENGR.			DEMULTIPLEXER
MATL. ENGR.			
RELIABILITY			
GR. ENGR.	1620	1/30/68	
PROJECT			
CUST. REP.	1620	1/30/68	SIZE D · CODE IDENT. NO. 04236 · 21164-122 · SCALE NONE · SHEET 1

REVISIONS				
SYM.	ZONE	DESCRIPTION	DATE	APPROVED

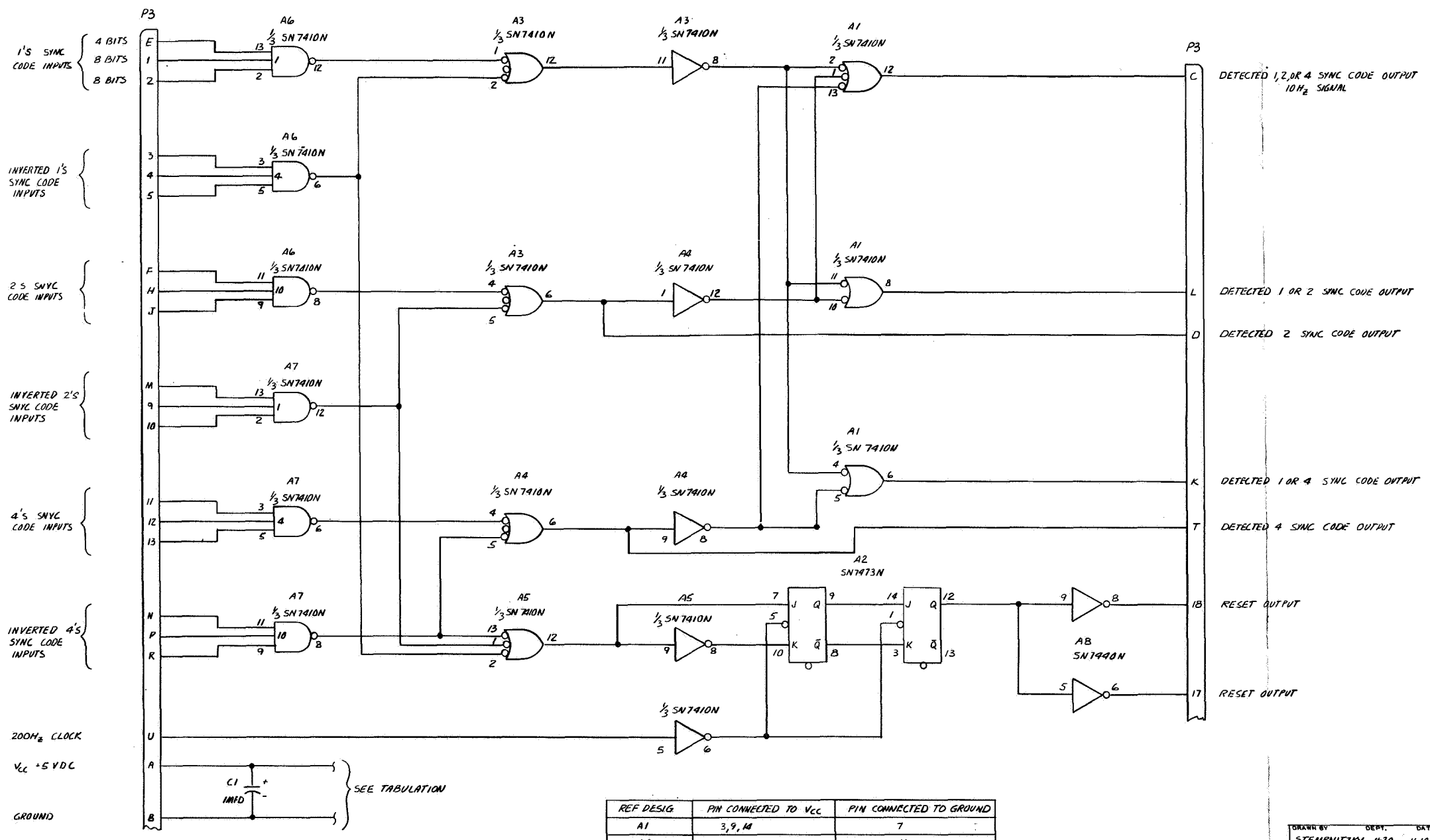


REF DESIG	Vcc CONN	GND CONN
A1 THRU A4	2 4 6	11
A5 THRU A10	14	7
A11	1,9,10,12,14	7
A12	2,5,10,12,14	7

DRAWN BY	DEPT.	DATE	MARTIN MARIETTA CORPORATION
STEMPNITZKY	1620	11-7-67	DENVER DIVISION P.O. BOX 179 DENVER, COLORADO
CHECKER N. Wellhoff		11-28-67	
STRESS ENGR.			SYNC CODE SHIFT REGISTER AND DECODER #2
WT. ENGR.			DEMULTIPLEXER
MATL. ENGR.			
RELIABILITY			
GR. ENGR. PROJECT Hollman	1620	1/30/68	SIZE D CODE IDENT. NO. 04236 21164-127
CUST. REP. R.K. Clause	1620	1/30/68	SCALE NONE SHEET 1

DEN 081607-01 (8-68)

REVISIONS				
SYM.	ZONE	DESCRIPTION	DATE	APPROVED
A		CHG'D CONNECTIONS TO A1 & A4	1-30-68 WKH.	



REF DESIG	PIN CONNECTED TO V_{CC}	PIN CONNECTED TO GROUND
A1	3, 9, 14	7
A2	2, 4, 6	11
A3	3, 9, 10, 13, 14	7
A4	2, 3, 10, 11, 13, 14	7
A5	3, 4, 10, 11, 14	7
A6-A7	14	7
A8	1, 2, 9, 10, 10, 12, 13, 14	7

DRAWN BY	DEPT.	DATE
STEMPNITZKY	1620	11-10-67
CHECKED W. Wellhoff		11-14-67
STRESS ENGR.		
WT. ENGR.		
MATL. ENGR.		
RELIABILITY		
GR. ENGR. G. A. Olsen	1620	1/29/68
PROJECT R. H. Clawson	1620	1/30/68
CUST. REP.		

MARTIN MARIETTA CORPORATION
DENVER DIVISION P.O. BOX 179
DENVER, COLORADO

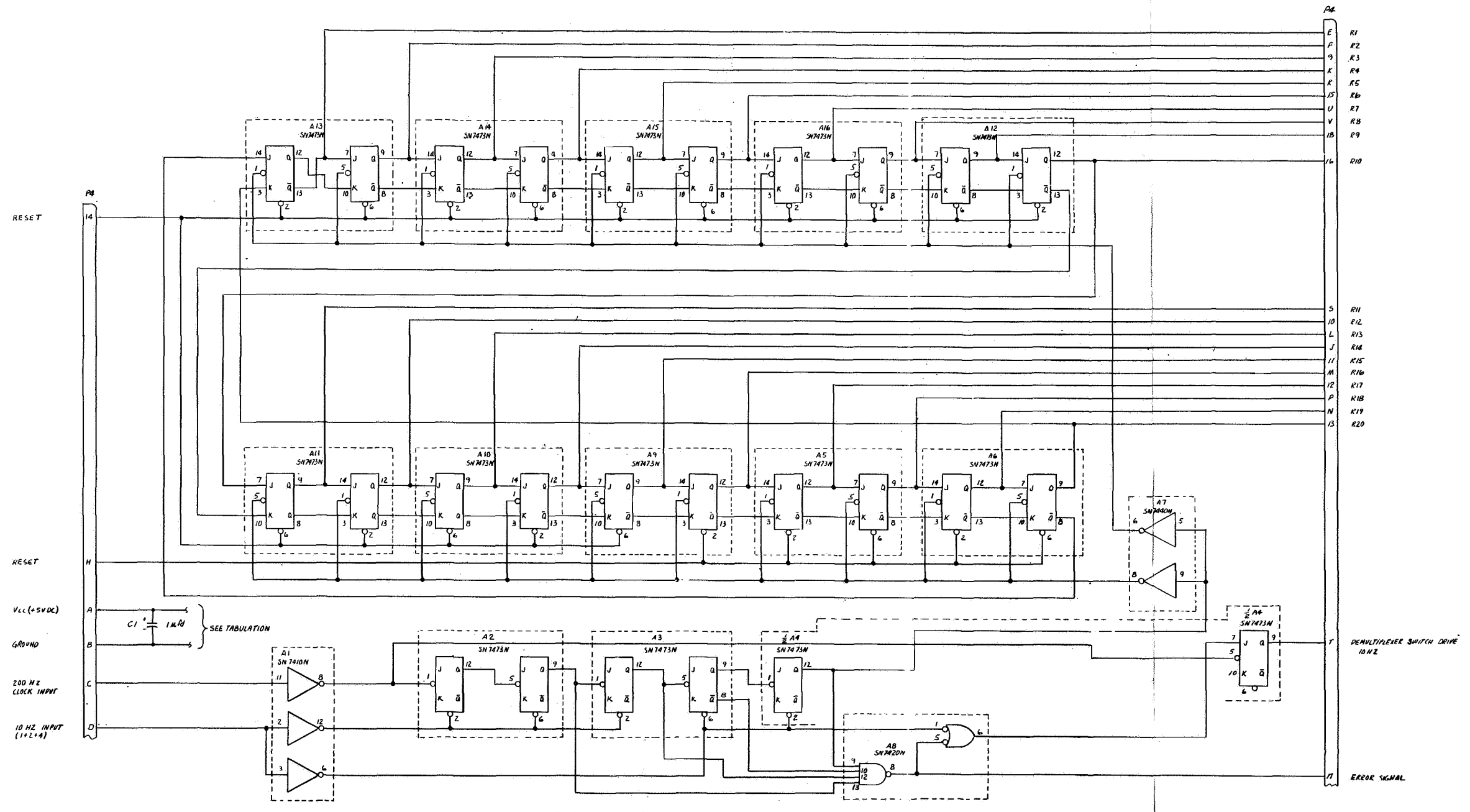
CHANNEL DECODER
DEMULTIPLEXER

SIZE	CODE IDENT. NO.	
D	04236	21164-123
CHG. A	SCALE NONE	SHEET 1

DEN 061607-01 18-661

FIGURE II-26

REVISIONS				
SYM	ZONE	DESCRIPTION	DATE	APPROVED
A		CNG'D CONNECTIONS ON A4	1-30-68	



REFERENCE DESIGNATION	PINS CONNECTED TO V_{CC}	PINS CONNECTED TO GROUND	TYPE
A1	1, 4, 5, 9, 10, 13, 14	7	SN7404N
A2, A3	3, 4, 7, 10, 14	11	SN7473N
A4	3, 4, 6, 14, 16	11	SN7473N
A5, A6 A9 THRU A16	4	11	SN7473N
A7	1, 2, 4, 10, 12, 13, 14	7	SN7440N
A8	2, 4, 14	7	SN7420N

DRAWN BY STEMPNITZKY 1620 10-20-67	DEPT.	DATE	MARTIN MARIETTA CORPORATION
CHECKED W. Wilhelm 10-25-67			DENVER DIVISION P.O. BOX 179 DENVER, COLORADO
STRESS ENGR.			
MT. ENGR.			SCHEMATIC DIAGRAM
MATL. ENGR.			SEQUENCE GENERATOR
RELIABILITY			
DR. ENGR. Robinson 1620 1/24/68			
PROJECT R.H. Clarner 1610 1/24/68	SIZE	CODE IDENT NO. 04236	21164-124
CUST. REP.	SCALE		SHEET 1

3. Demultiplexing

Demultiplexing is accomplished by two DPDT relays and the associated logic shown in Figures II-28 and II-29 and the output OR gates shown in Figure II-26.

a. Subchannel decoder - The 2 and 4 outputs from the sync word decoder are ORed with the 1 output to produce four outputs in Figure II-26 of 1 OR 2, 2, 1 OR 4 and 4. These are gated by the R_n selected by the rotary switch to either the set or reset inputs of the cross-coupled gate flip-flops. One flip-flop is set for a 2 input and the other for a 4 input; both are reset for a 1 input.

R_n is also used to gate the 10 Hz demultiplexer drive signal into a two stage counter that is synchronized every 8 seconds by the reset pulse.

The waveforms of the two cross-coupled gate flip-flops, A6 and A7, and the two counter stages, A1-1 and A1-2, are shown in Figure II-29. Since the counter input is gated by R_n, the counter stages A1-1 and A1-2 change state simultaneously with any commutation of the subchannels that could occur on that channel.

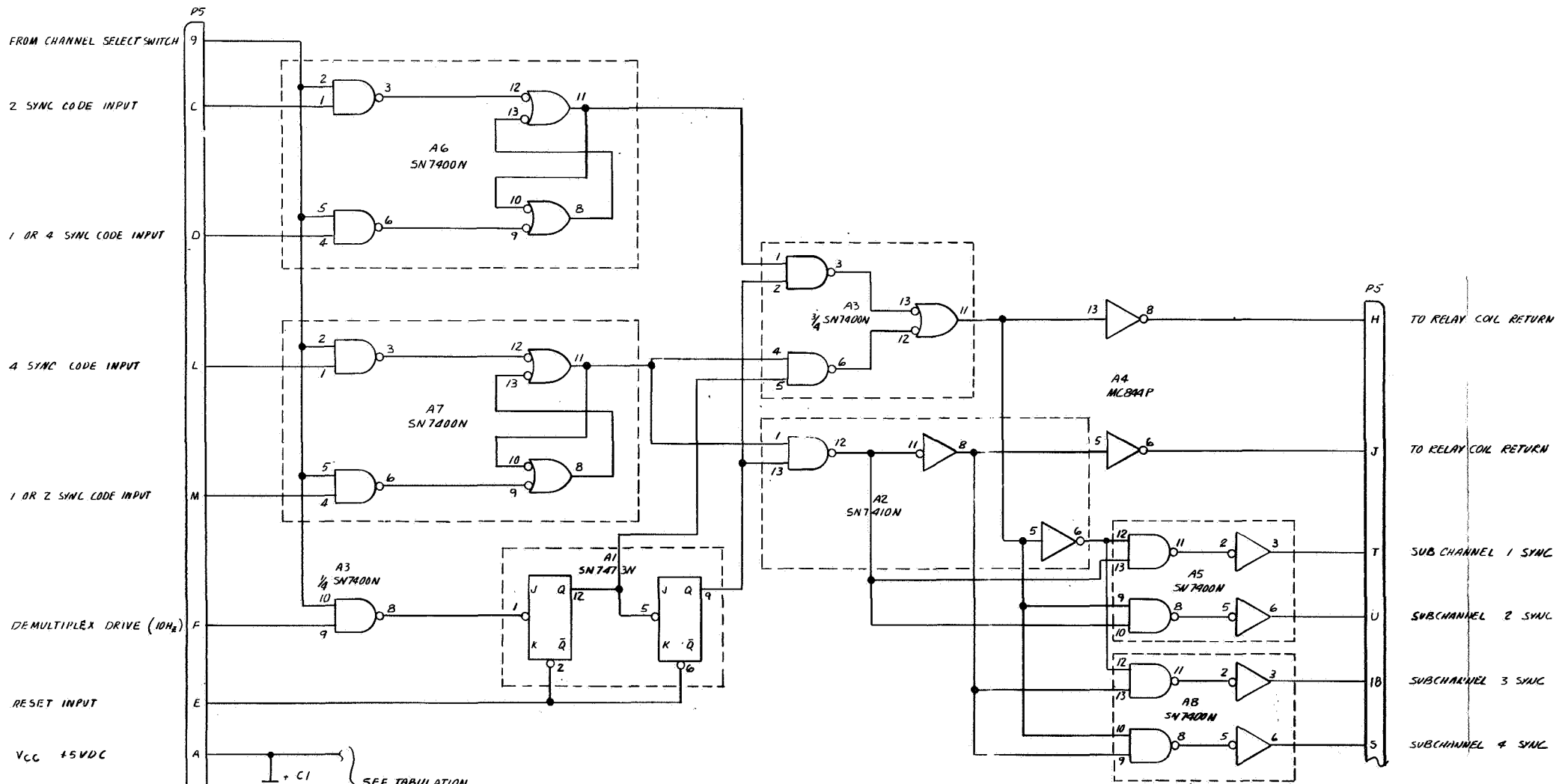
The 20 channel signal inputs are connected to the other deck of the three rotary switches in the same sequence as the R_n signals so that R1 corresponds to channel 1 and so on to where R20 corresponds to channel 20.

b. Switching - A1-1 and A1-2 operate in synchronism with the selected channel commutation. There are three possible conditions for A6 and A7: both reset, A6 only set and A7 only set corresponding to a single subchannel, 2 subchannels and 4 subchannels. If both are reset, neither relay operates and the selected channel is always connected to the subchannel "a" output and subchannel "a" sync is always positive. If A6 is set and A7 reset corresponding to a 2 subchannel signal, relay K1, Figure II-30, never operates and K2 is energized in the sxcond half of each 8 second cycle for channel A and similarly for B and C. Thus the selected channel is connected to the subchannel "a" output during the first 4 seconds of the cycle and the subchannel "b" output during the last 4 seconds. Subchannel "a" and "b" sync outputs are positive in the first and second halves of the cycle respectively. In a similar manner, when A6 is reset and A7 is set indicating a 4 subchannel channel, the relays connect the signal to subchannels "a", "b", "c" and "d" in sequence and their respective sync outputs are positive in the same sequence. The waveforms for 1, 2 and 4 subchannels are shown in Figure II-29.

4. Power Supply

The power supply for the demultiplexer is a packaged power supply, Technipower Model P-5.1-3.0 that provides 3 amps at +5 V dc from the 117 volt, single phase, 60 Hz line. A high power zener diode and a line fuse are used for over voltage protection of the circuitry.

REVISIONS				
SYM.	ZONE	DESCRIPTION	DATE	APPROVED
A		ON P5 18 WAS V	1-30-68 WEN	



REF DESIG	PIN CONNECTED TO V_{CC}	PIN CONNECTED TO GND
A1	3,9,7,10,14	11
A2	2,3,4,9,10,14	7
A3, A6, A7	14	7
A4	1,2,4,9,10,12,14	7
A5, A8	1,4,14	7

DRAWN BY	DEPT.	DATE
STEMPNITZKY	1620	11-10-67
CHECKER		11-16-67
STRESS ENGR.		
WT. ENGR.		
MATL. ENGR.		
RELIABILITY		
GR. ENGR.		
PROJECT		
CUST. REP.		

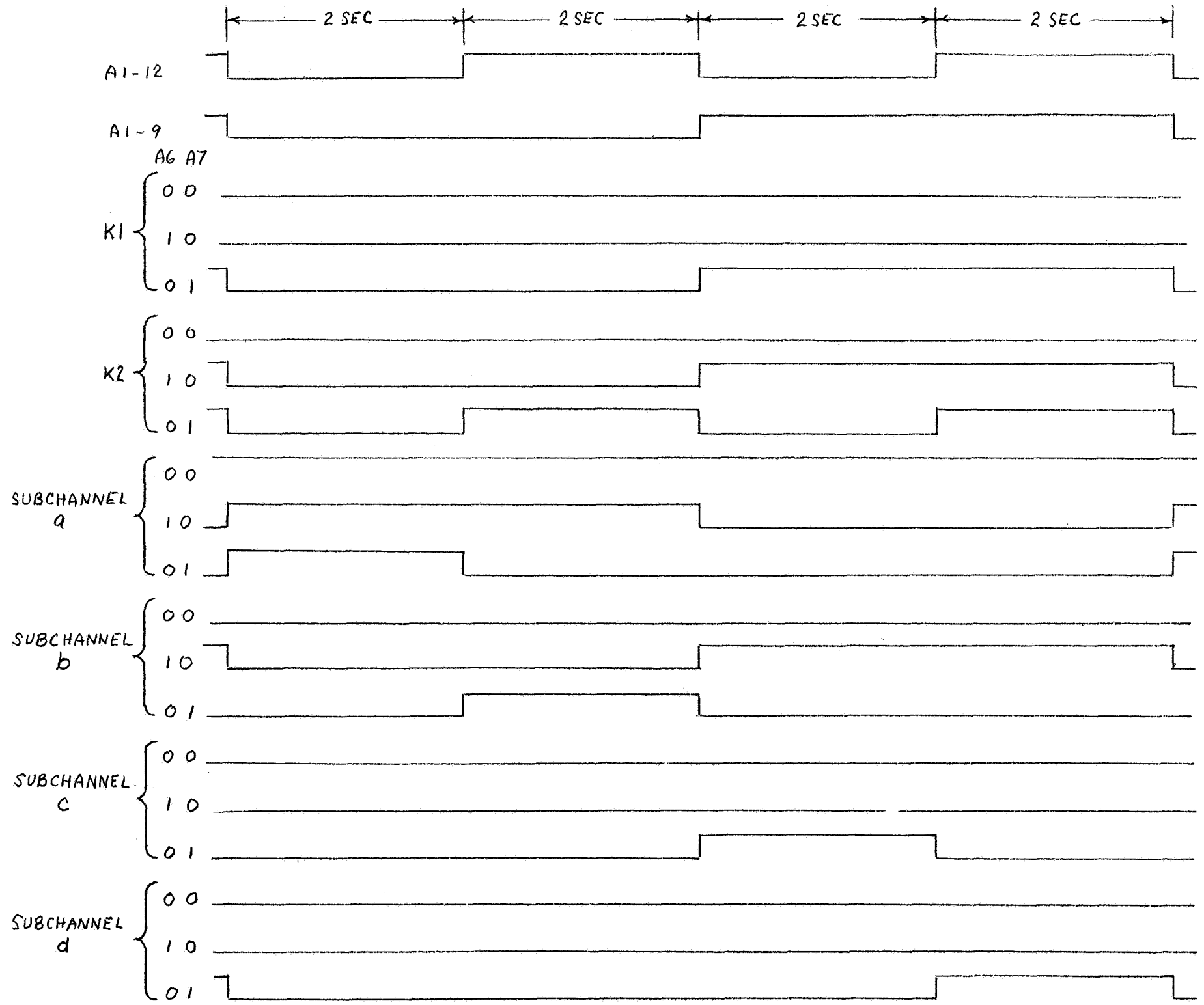
MARTIN MARIETTA CORPORATION
DENVER DIVISION P.O. BOX 179
DENVER, COLORADO

SWITCH
DEMULTIPLEXER

SIZE	CODE IDENT. NO.	
D	04236	21164-125
SCALE NONE		SHEET 1
CHG. A		

DEN 081807-01 18-681

FIGURE II-28

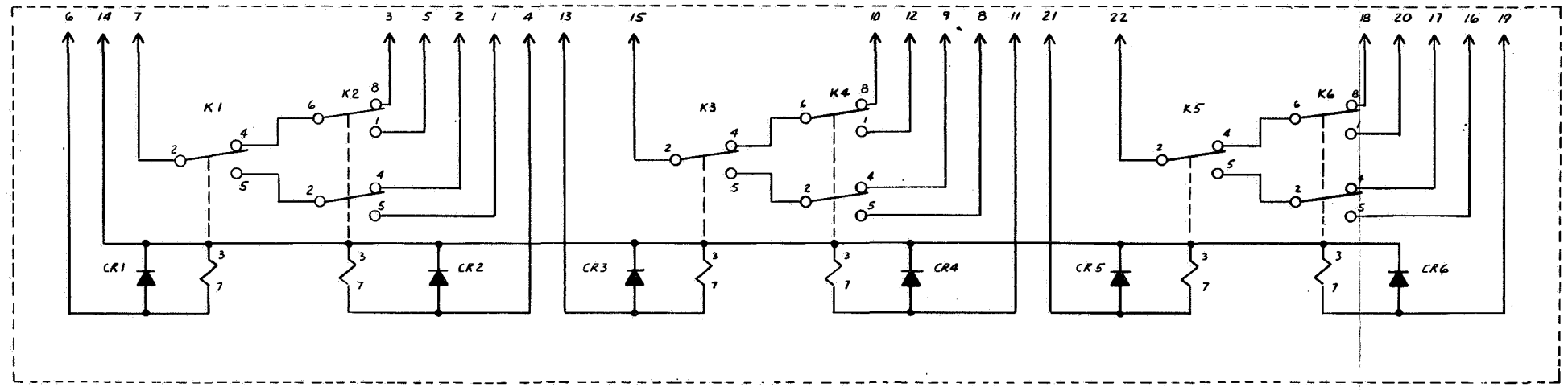


SYNC CODE	A6-11	A7-11
1	0	0
2	1	0
4	0	1

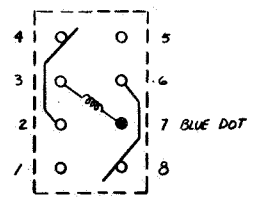
FIGURE II-29

DEMULTIPLEXER CHANNEL DECODER WAVEFORMS

REVISIONS				
SYM.	ZONE	DESCRIPTION	DATE	APPROVED



RELAY - PIN VIEW
(TYP.)



DRAWN BY	DEPT.	DATE
STEMPNIT2KY	1620	11-4-67
CHECKER		11-10-67
STRESS ENGR.		
WT. ENGR.		
MATL. ENGR.		
RELIABILITY		
GR. ENGR. PROJECT		1/26/68
R16 Clarke	1610	1/24/68
CUST. REP.		
CHG.		

MARTIN MARIETTA CORPORATION
DENVER DIVISION P.O. BOX 179
DENVER, COLORADO

RELAY BOARD
DEMULTIPLEXER

SIZE	CODE IDENT. NO.	
D	04236	21164-126
SCALE NONE		SHEET 1

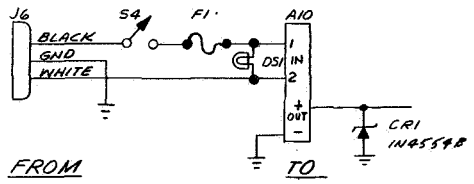
DEN 061607-01 (8-66)

FIGURE II-30

REVISIONS				
SYM	ZONE	DESCRIPTION	DATE	APPROVED
A		GENERAL REVISIONS	1-24-68	

POWER & GROUND CONNECTIONS

FROM	TO
VCC (A10 OUT +)	J1-A
J1-A	J2A-A
J2A-A	J2B-A
J2B-A	J3-A
J3-A	J4-A
J4-A	J5A-A
J5A-A	J5B-A
J5B-A	J5C-A
VCC (A10 OUT +)	A9-14 & C1 +
GND (A10 OUT -)	J1-B
J1-B	J2A-B
J2A-B	J2B-B
J2B-B	J3-B
J3-B	J4-B
J4-B	J5A-B
J5A-B	J5B-B
J5B-B	J5C-B
GND (A10 OUT -)	C1 -



FROM	TO
J1-N	TP4, J2A-12, J2B-12, J3-U, J4-C
J1-R	J2A-R
J1-6	J2A-6
J1-T	J3-E
J1-18	J3-3
J1-S	J3-F
J1-U	J3-M
J1-K	J3-11
J1-V	J3-N
J1-P	J2A-E
J2A-3	J3-1
J2A-V	J3-4
J2A-C	J3-H
J2A-U	J3-9
J2A-D	J3-12
J2A-T	J3-P
J2A-R	J2B-6
J2A-S	J2B-E
J2B-3	J3-2
J2B-V	J3-5
J2B-C	J3-J
J2B-U	J3-10
J2B-D	J3-13
J2B-T	J3-R
J3-C	J4-D
J3-L	J5A-M, J5B-M, J5C-M
J3-D	J5A-C, J5B-C, J5C-C
J3-K	J5A-D, J5B-D, J5C-D
J3-T	J5A-L, J5B-L, J5C-L
J3-18	J4-14
J3-17	J4-H, J5A-E, J5B-E, J5C-E

FROM	TO.
J4-E	S1A-1, S2A-1, S3A-1
J4-F	2 2 2
J4-9	3 3 3
J4-K	4 4 4
J4-R	5 5 5
J4-15	6 6 6
J4-U	7 7 7
J4-V	8 8 8
J4-18	9 9 9
J4-16	10 10 10
J4-S	11 11 11
J4-10	12 12 12
J4-L	13 13 13
J4-J	14 14 14
J4-11	15 15 15
J4-M	16 16 16
J4-12	17 17 17
J4-P	18 18 18
J4-N	19 19 19
J4-13	S1A-20, S2A-20, S3A-20
J4-T	J5A-F, J5B-F, J5C-F
J5A-9	S1A-C
J5B-9	S2A-C
J5C-9	S3A-C
J5A-H	A9-4
J5B-H	A9-11
J5C-H	A9-19
J5A-J	A9-6
J5B-J	A9-13
J5C-J	A9-21

FROM	TO
J7-a	S1B-1, S2B-1, S3B-1
J7-b	2 2 2
J7-c	3 3 3
J7-d	4 4 4
J7-e	5 5 5
J7-f	4 6 6
J7-g	7 7 7
J7-h	8 8 8
J7-i	9 9 9
J7-j	10 10 10
J7-k	11 11 11
J7-n	12 12 12
J7-p	13 13 13
J7-g	14 14 14
J7-X	15 15 15
J7-Y	16 16 16
J7-Z	17 17 17
J7-A	18 18 18
J7-B	19 19 19
J7-C	S1B-20, S2B-20, S3B-20
J7-D	J1-J
A9-7	S1B-C, TP1
A9-15	S2B-C, TP2
A9-22	S3B-C, TP3
J7-E	J5B-B

FROM	TO
J8-a	A9-3
J8-b	A9-5
J8-c	A9-2
J8-d	A9-1
J8-e	J5A-T
J8-f	J5A-U
J8-g	J5A-18
J8-h	J5A-S
J8-j	A9-10
J8-j	A9-12
J8-k	A9-9
J8-m	A9-8
J8-n	J5B-T
J8-p	J5B-U
J8-g	J5B-18
J8-r	J5B-S
J8-s	A9-18
J8-t	A9-20
J8-X	A9-17
J8-Y	A9-16
J8-Z	J5C-T
J8-A	J5C-U
J8-B	J5C-18
J8-C	J5C-S
J8-D	J4-17
J8-E	J5B-B

DRAWN BY	DEPT.	DATE	MARTIN MARIETTA CORPORATION
E. MARTINEZ	1620	11-22-67	DENVER DIVISION P.O. BOX 179 DENVER, COLORADO
CHECKED		11-27-67	
STRESS ENGR.			INTERCONNECTIONS DIAGRAM- DEMULTIPLEXER
WT. ENGR.			
MATL. ENGR.			
RELIABILITY			
DR. ENGR.		11-27-67	SIZE F CODE IDENT NO. 38597 DWG NO. 21164-120
PROJECT			SCALE SHEET 1 OF 1
CUST. REP.			DWG A

5. Interconnections

The demultiplexer interconnections are made by point-to-point wiring between the pc board receptacles and to all other points. The interconnections are shown schematically in Figure II-31.

III. MECHANICAL CONSTRUCTION

A. MULTIPLEXER

The multiplexer is packaged in a welded aluminum case with outside dimensions of 10.58 in. long, 5.88 in. wide, and 6.18 in. high. Its total displaced volume is approximately 350 cu. in. and it weighs approximately 10 ¼ lb. The mounting hole pattern is a 6-in. by 8-in. rectangle.

A top view of the multiplexer with the cover removed is shown in Figure III-1. Four of the plug-in modules are in fixed positions and contain the power supply, A14, the sync code generator OR gates, A13, the sync code generator, A12, and the sequence generator A11, and are plugged into J14, J13, J12, and J11, respectively, of the mother board. The remaining receptacles in the mother boards, J1 through J10, can each have a dual 1 subchannel, a dual 2 subchannel, or a dual 4 subchannel switch plug-in module installed in positions A1 through A10 respectively. The channel numbers associated with each position are: A1, 19 and 20; A2, 17 and 18; A3, 15 and 16; A4, 13 and 14; A5, 11 and 12; A6, 9 and 10; A7, 7 and 8; A8, 5 and 6; A9, 3 and 4; and A10, 1 and 2. Since the dual subchannel plug-ins are interchangeable, any two channels can have two, four, or eight subchannels time multiplexed on their outputs as desired with the plug-ins available.

Each channel will, as described above, time multiplex onto its output subchannel input signals ranging in frequency from dc to 3,000 Hz and in voltage level from +2.5 volts to -2.5 volts (5 volts peak-to-peak) with respect to signal common.

B. DEMULTIPLEXER

The demultiplexer is constructed on a 17-in. long, 8-in. wide by 2-in. deep aluminum chassis. The aluminum front panel is a standard 8 3/4-in. panel for a 19-in. rack. Mounted on top of the chassis is a packaged power supply and a card cage. The card cage is mounted over a chassis cutout and all interconnecting wires, except those to the front panel switches, are run inside the chassis. The printed circuit card receptacles are offset in the card guides to prevent reversal of the cards in the receptacles.

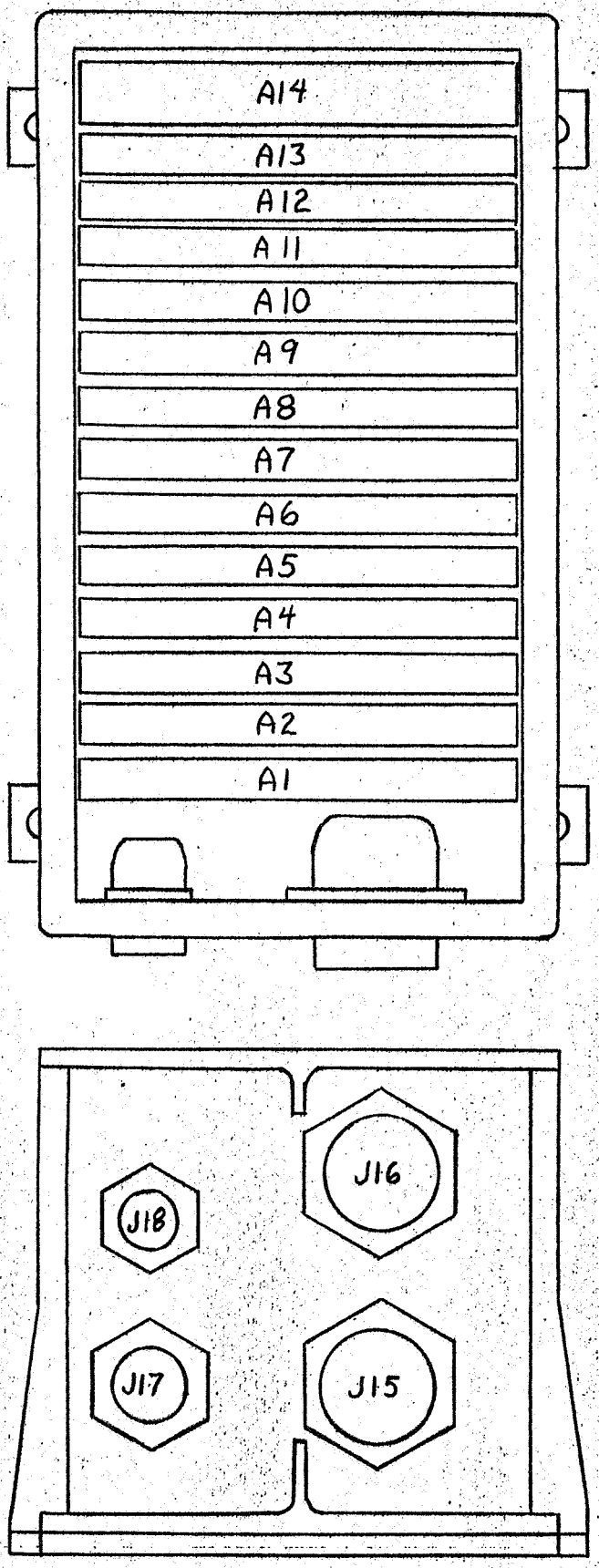


FIGURE III-1
MULTIPLEXER, FRONT AND TOP VIEWS, COVER REMOVED

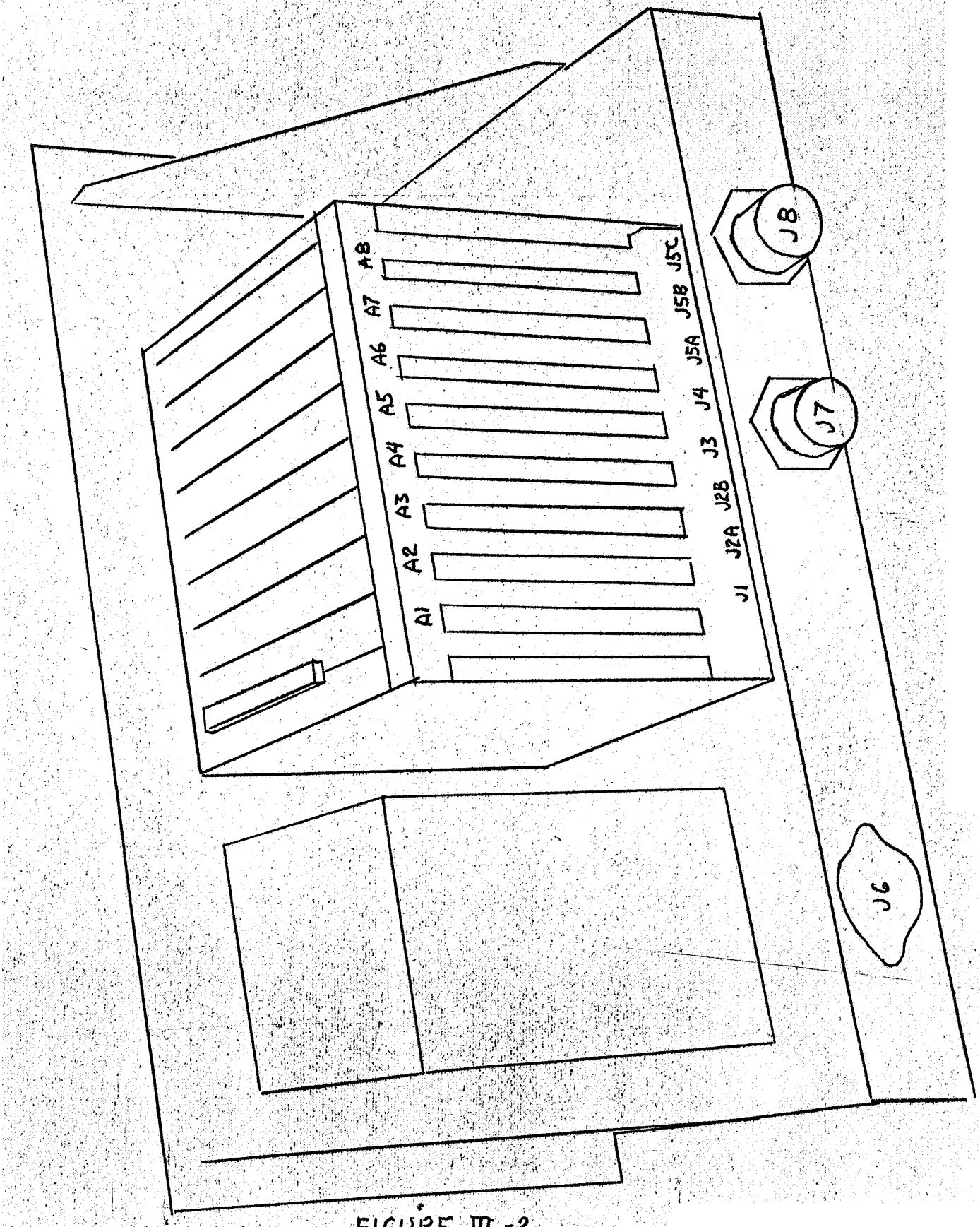


FIGURE III-2
DEMULTIPLEXER, REAR VIEW

Figure III-2 is a rear view of the demultiplexer. Input connector J7 and output connector J8 are located on the rear of the chassis along with input power connector J6 and the fuse holder.

The card cage was designed with an extra position used to store the extender card necessary for any trouble-shooting of the plug-in boards.

The sync code shift register and clock regenerator board P1 plugs into J1. The sync code shift register and decoder boards P2A and P2B plug into J2A and J2B. The channel decoder board P3 plugs into J3 and the sequence generator P4 plugs into J4.

The three channel demultiplexer switches, P5A, P5B, and P5C, are interchangeable and plug into J5A, J5B and J5C. The above switches drive an array of six DPDT relays mounted on a printed circuit board under the chassis. These relays are the actual signal decommutating switches.

IV. APPLICATIONS CONSIDERATIONS

A. MULTIPLEXER

There are two things that must be considered when using the multiplexer. The first is that the capacitance of the cable used to connect the sensors to the multiplexer will alter the frequency response by altering the apparent input impedance for various frequencies. As an example, if a cable has 30 picofarads per foot between the signal lead and the signal common, and there is ten feet of cable between the sensor and the multiplexer, the shunt capacitance will be 300 picofarads. The equivalent impedance at 1500 Hz is 353 kohms. This makes the apparent impedance of the sensor only 78 k ohms. The impedance at the sensor for frequencies close to dc will still be 100 k ohms. The longer the cable or the more capacitance per foot from the signal lead to the common lead, the more pronounced this effect will be.

The second consideration in the use of the multiplexer is grounding. Any current flowing in the signal input common will produce a voltage at the signal input that will look like a signal to the multiplexer. This effect showed up several times during testing of the multiplexer. During vibration testing a 5 millivolt offset was generated by currents between the shaker and the other test equipment. However, the largest effect encountered was only about 25 millivolts or 1% of the 2.5 volt peak signal.

B. DEMULTIPLEXER

The demultiplexer chassis is connected to signal ground through the protective zener diode. If this produces grounding problems in use, it should be isolated with appropriate hardware.

The demultiplexer is sensitive to noise spikes on the sync code input. The effect of the noise spikes is for the demultiplexer to lose sync. It may be necessary to use a low pass filter on the sync code input.